WARP: Physical Layer Design

Patrick Murphy & Sid Gupta

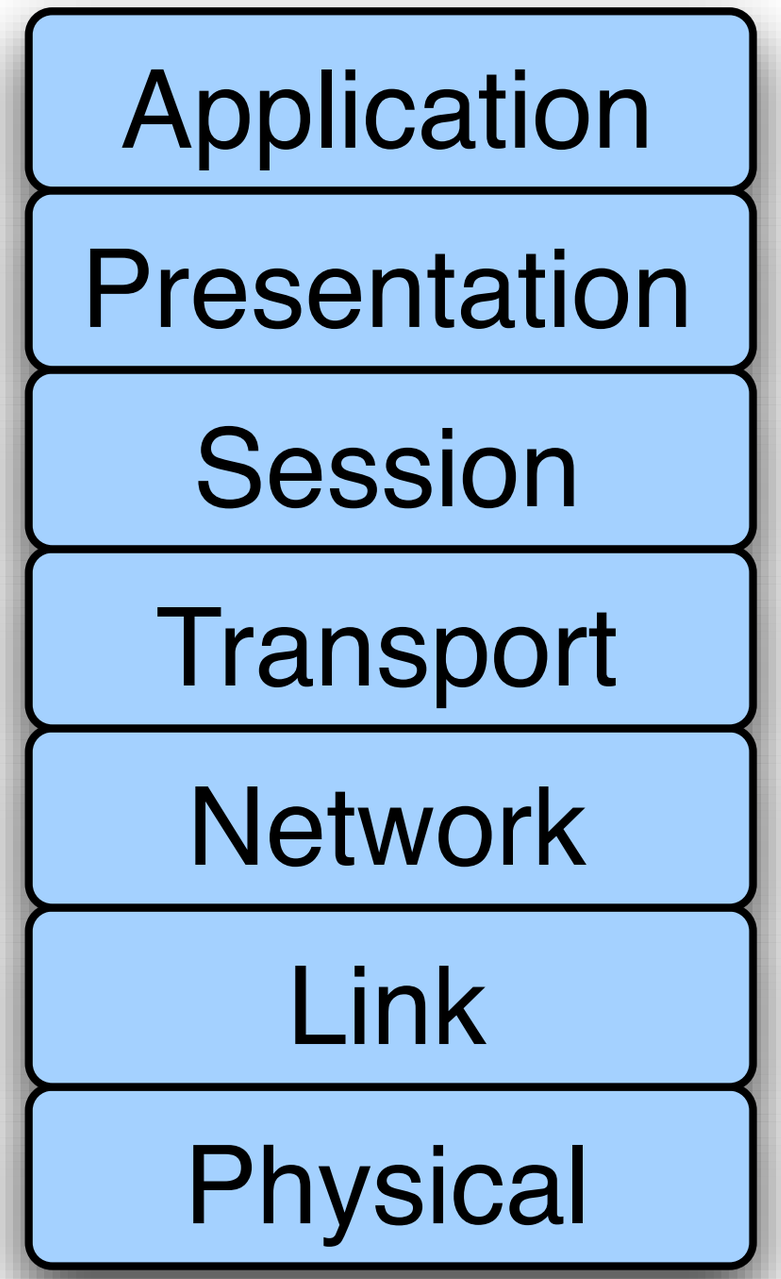
WARP Workshop
Rice University
March 29, 2010

Questions From Labs 1 & 2?

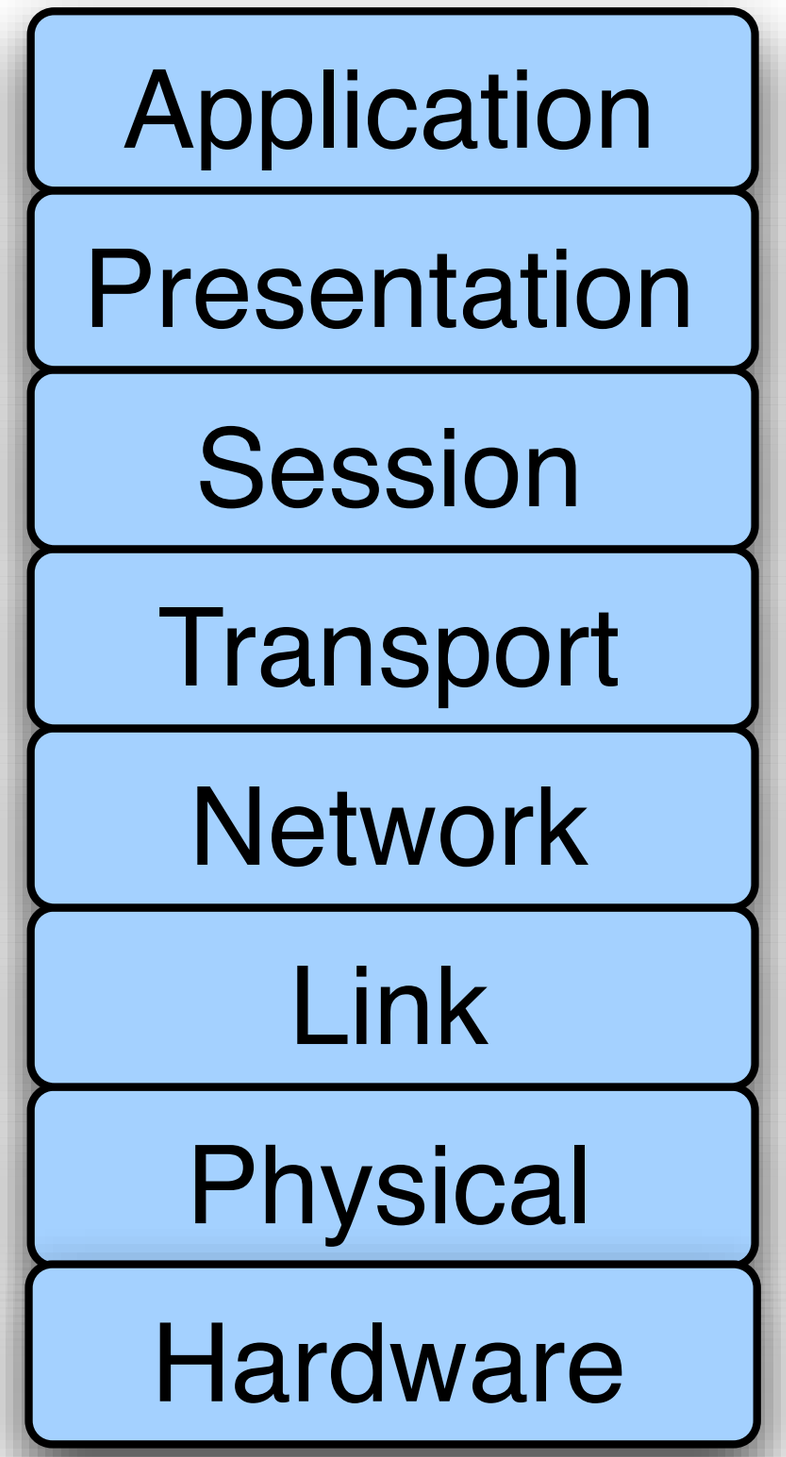
PHY Design - Outline

- Physical Layer Overview
- Integrating Physical Layer Designs
- Lab 3: Building a Simple Transceiver

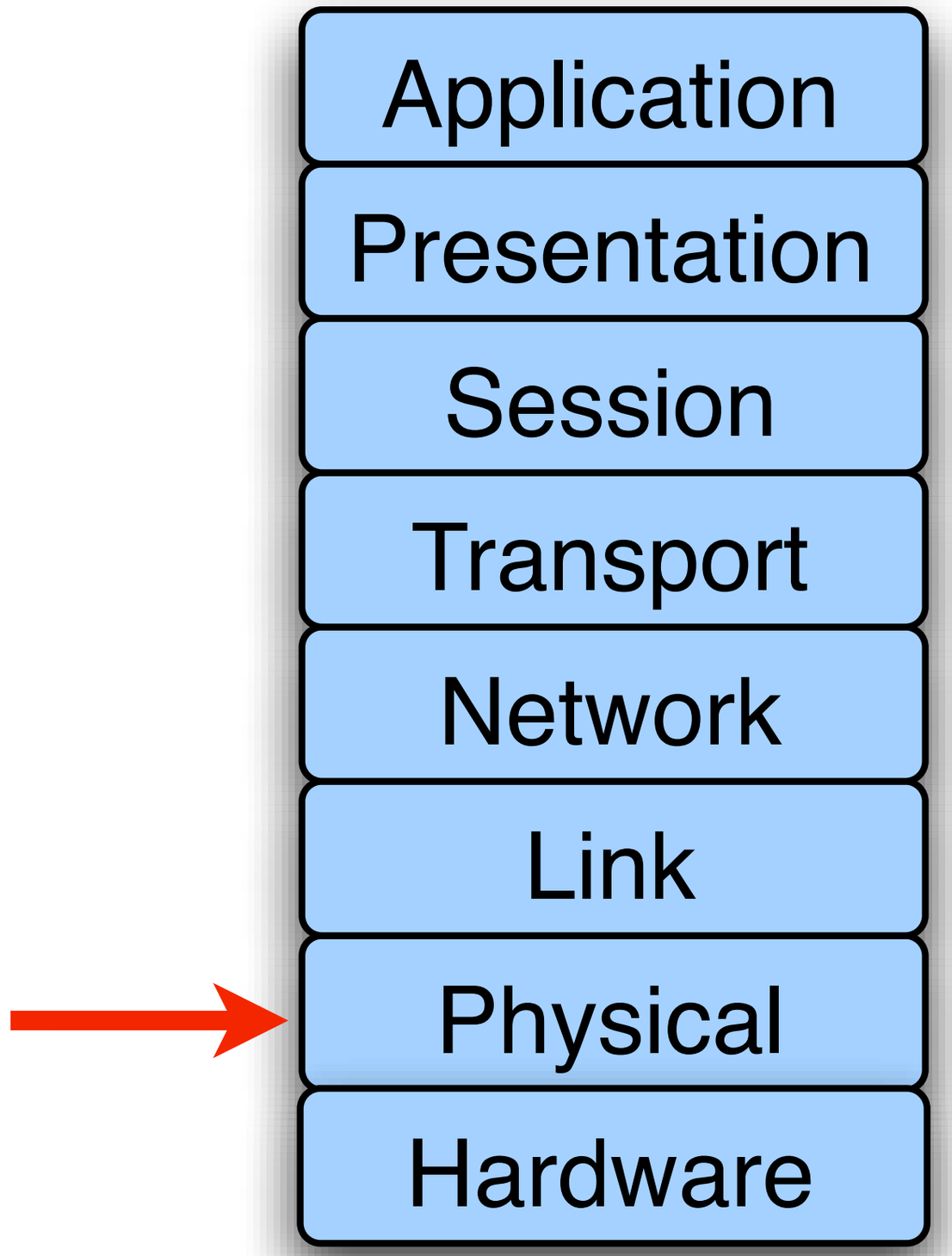
Physical Layer Basics



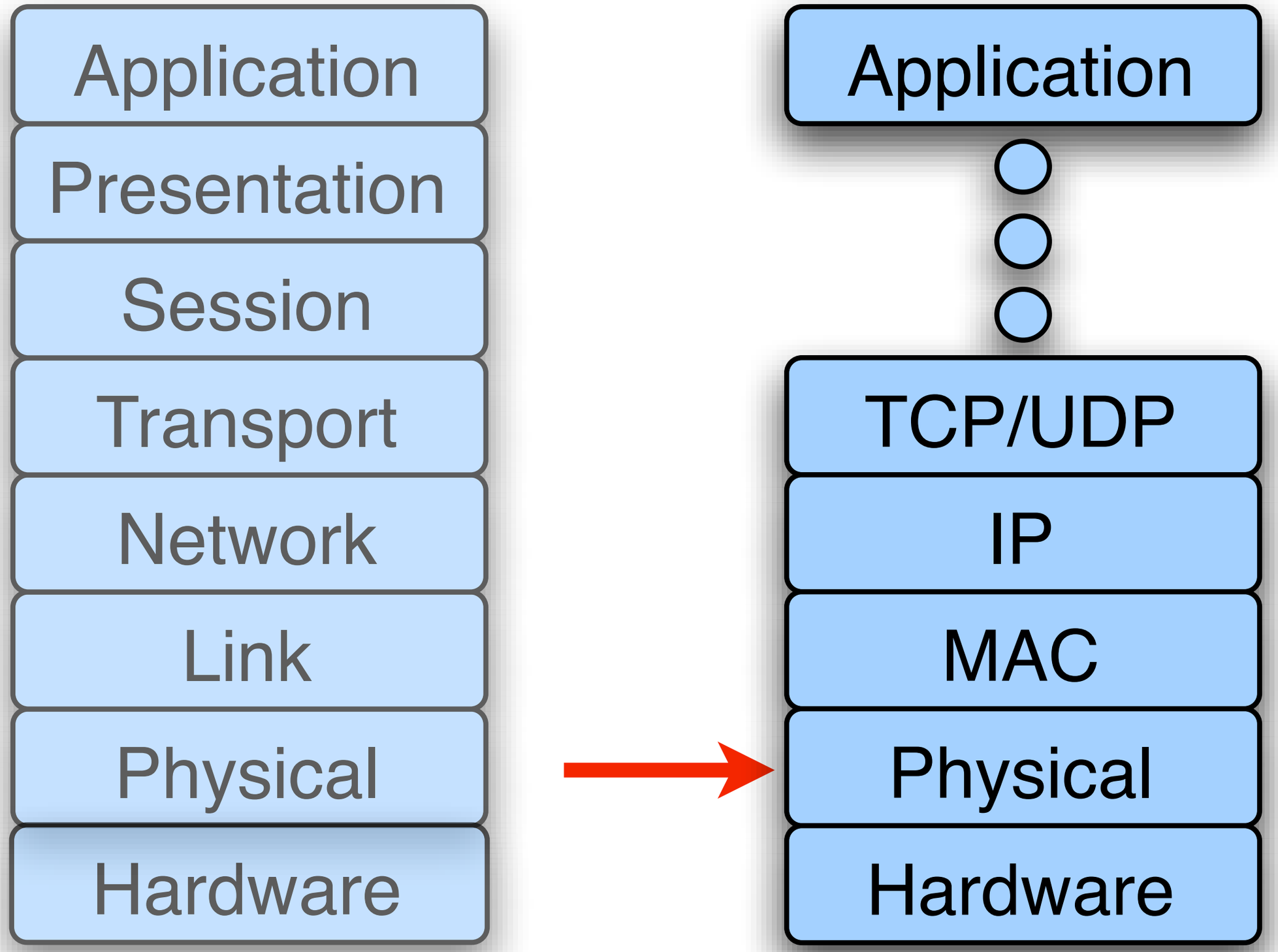
Physical Layer Basics



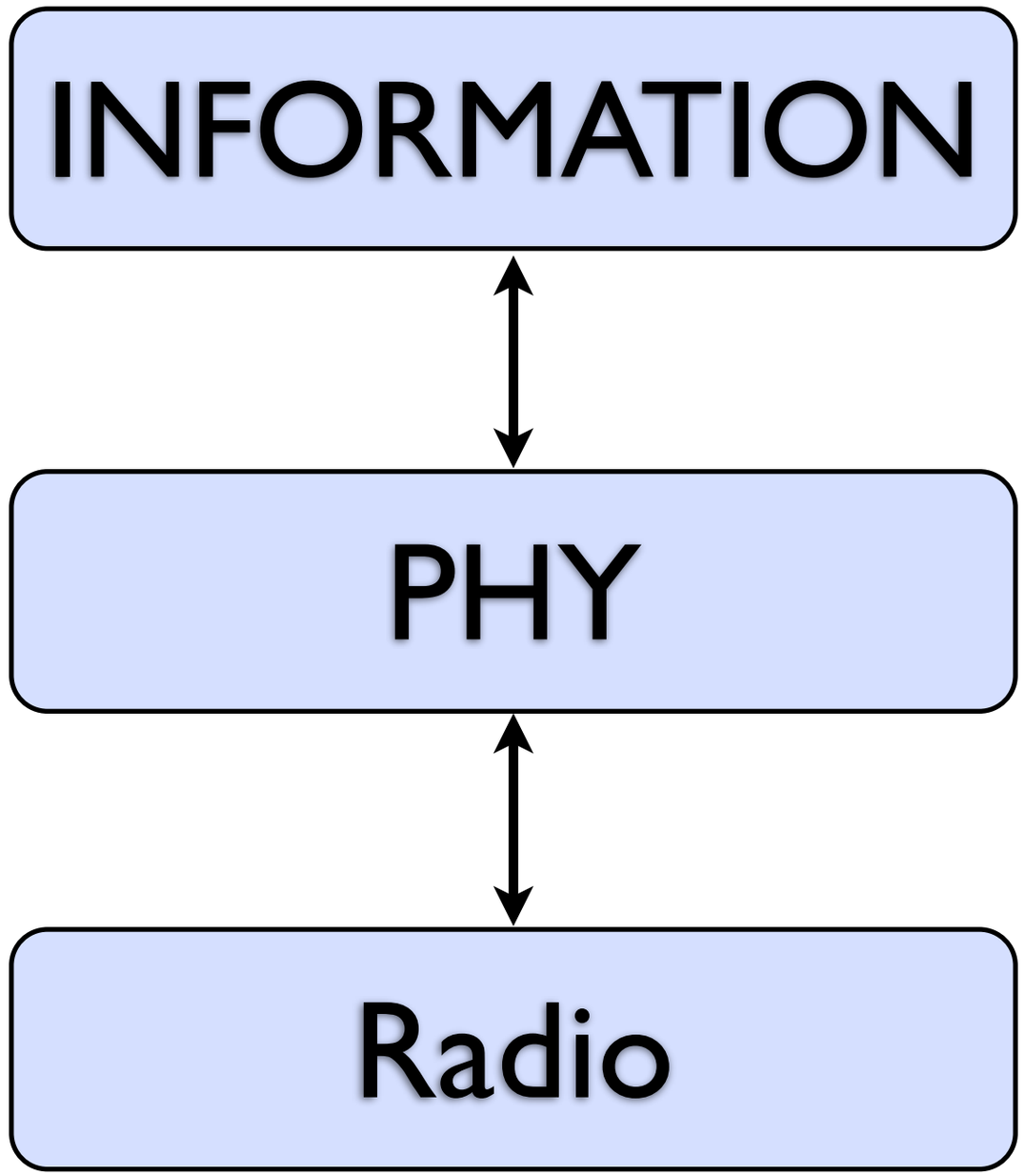
Physical Layer Basics



Physical Layer Basics



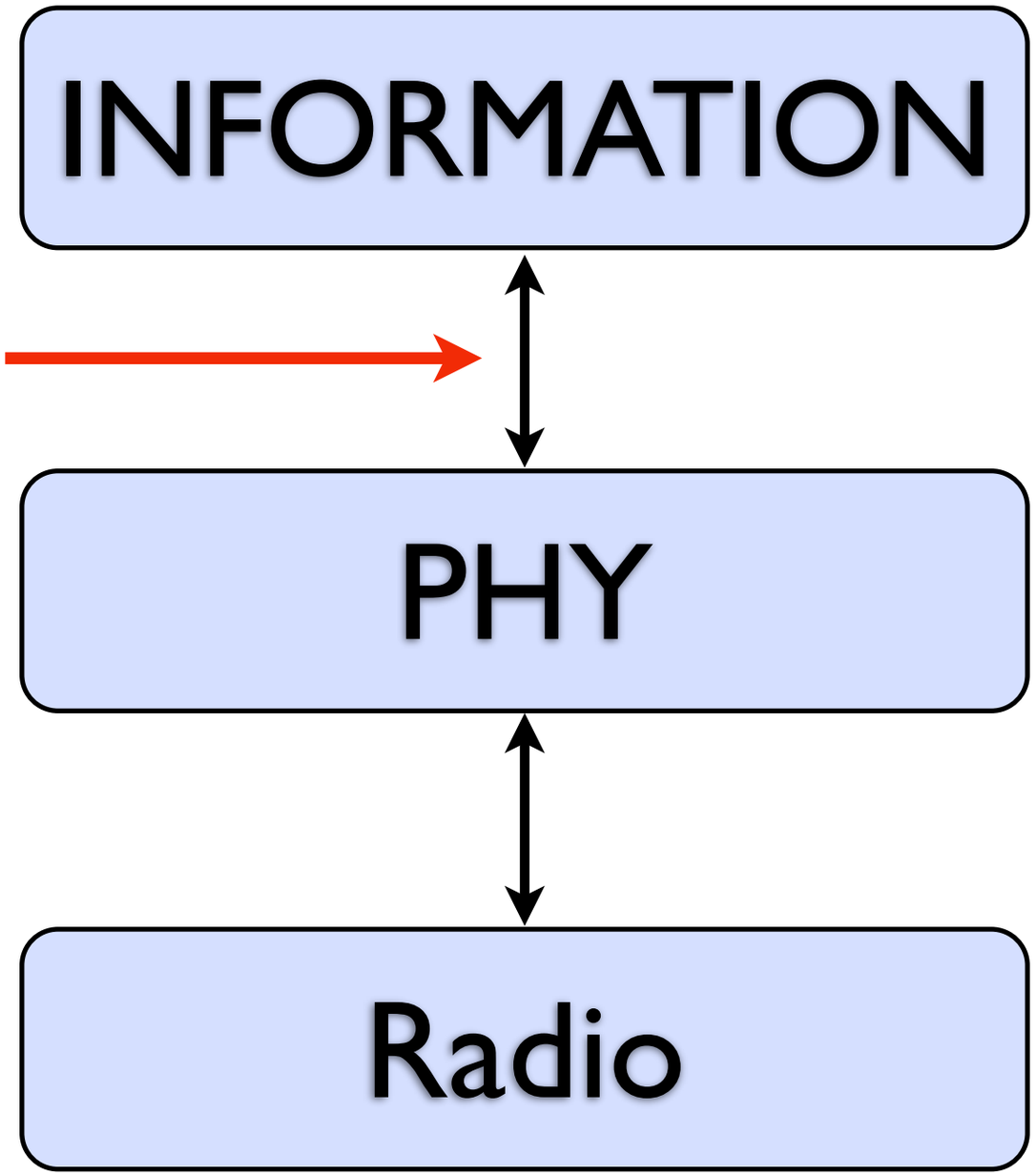
Physical Layer Basics



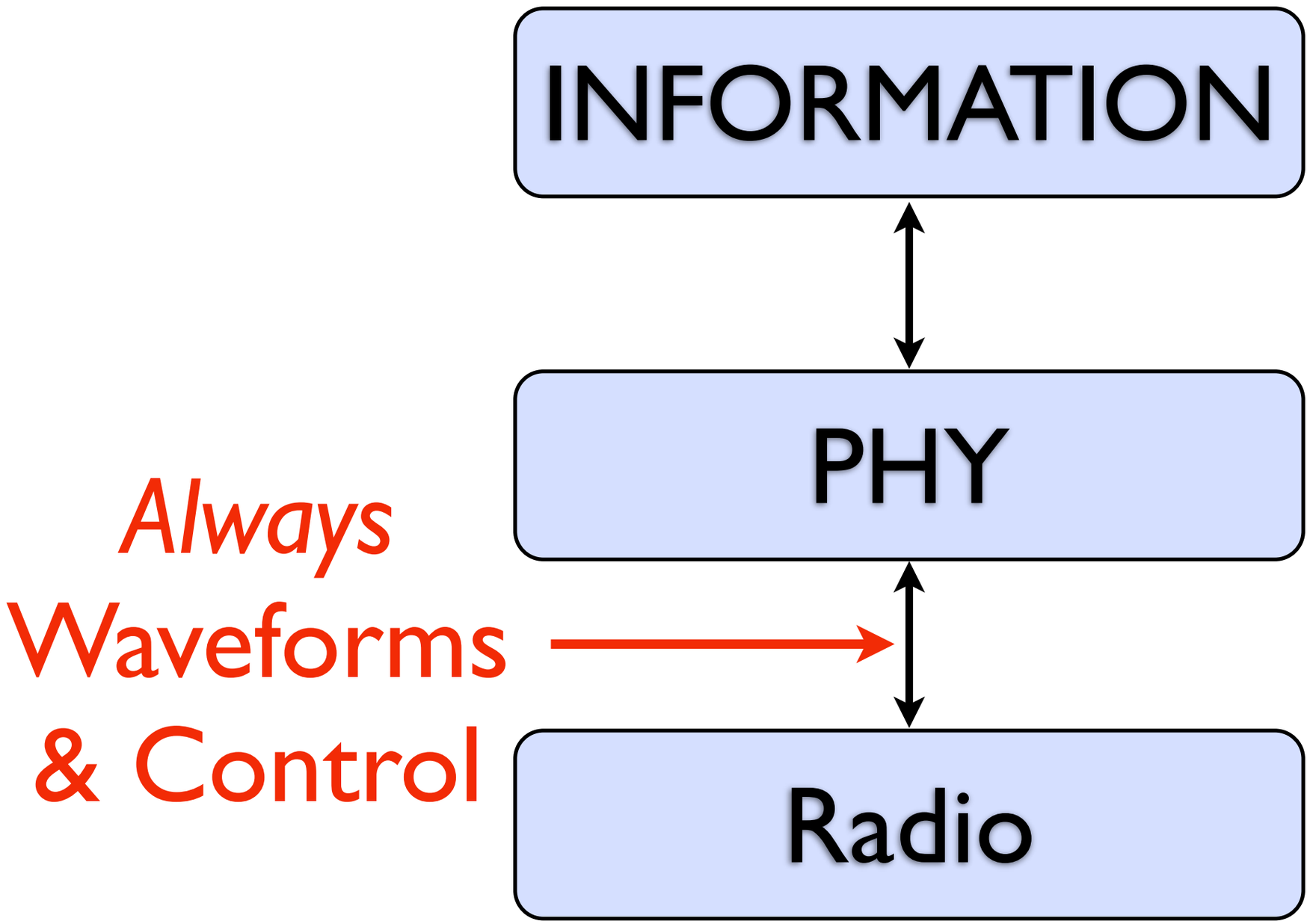
Physical Layer Basics

Application Dependent

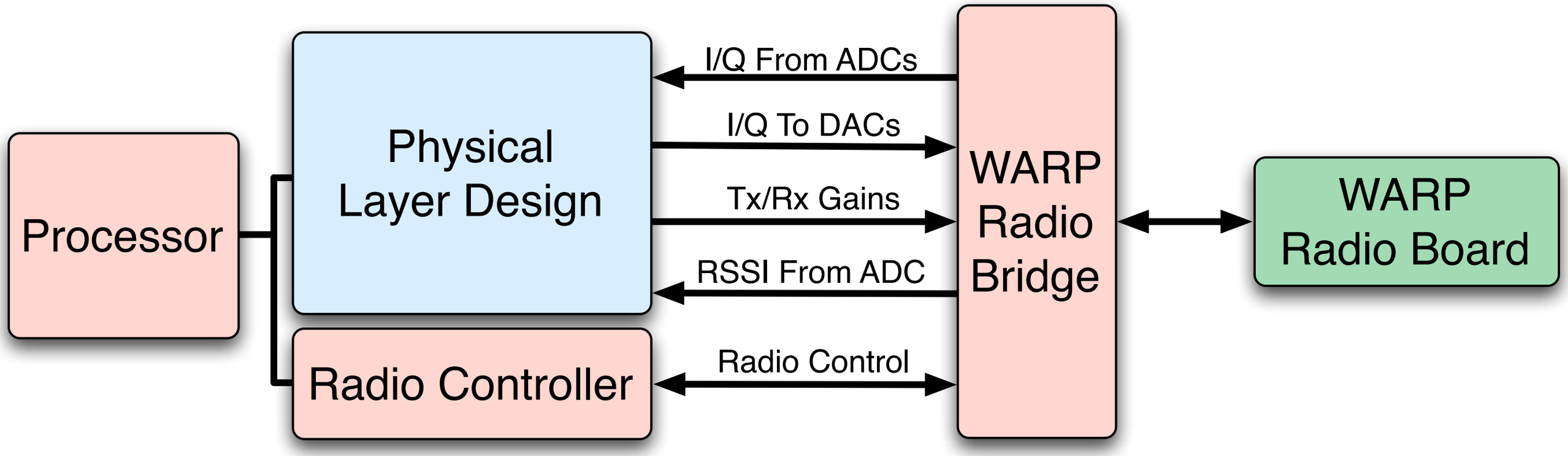
(Bytes, Packets, Waveforms, etc.)



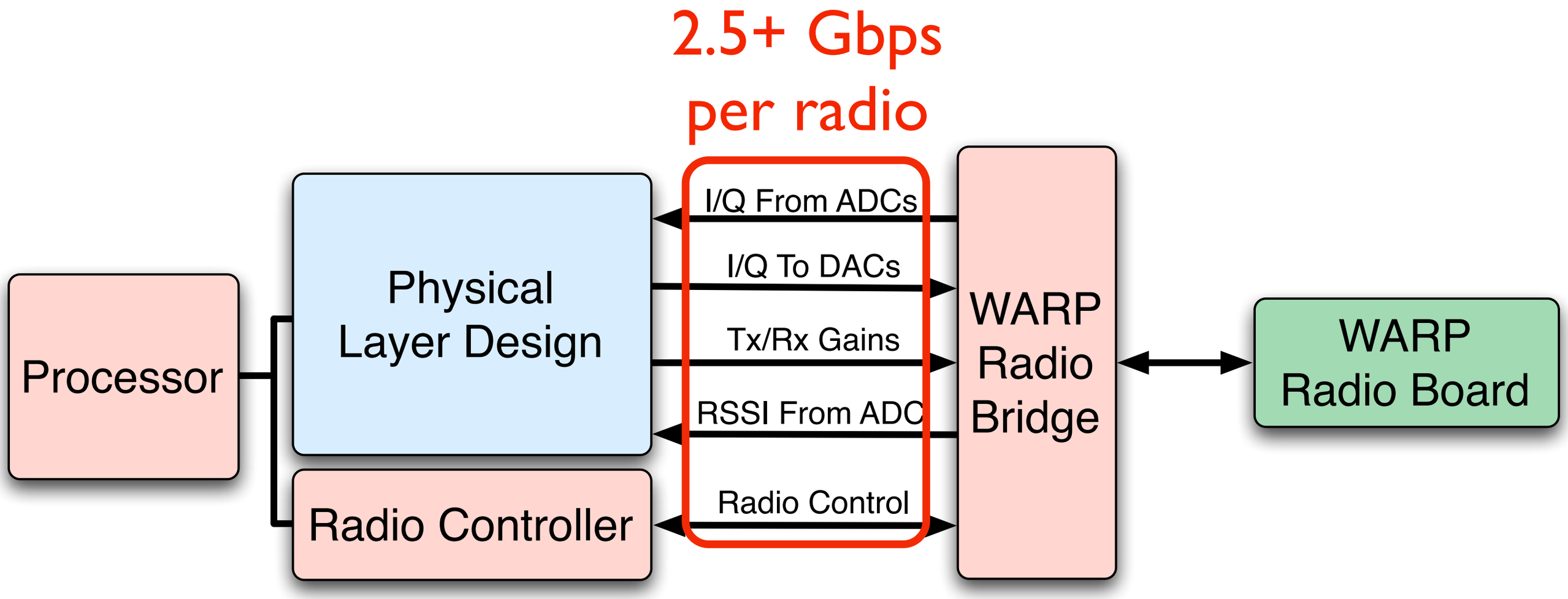
Physical Layer Basics



Physical Layer in Hardware

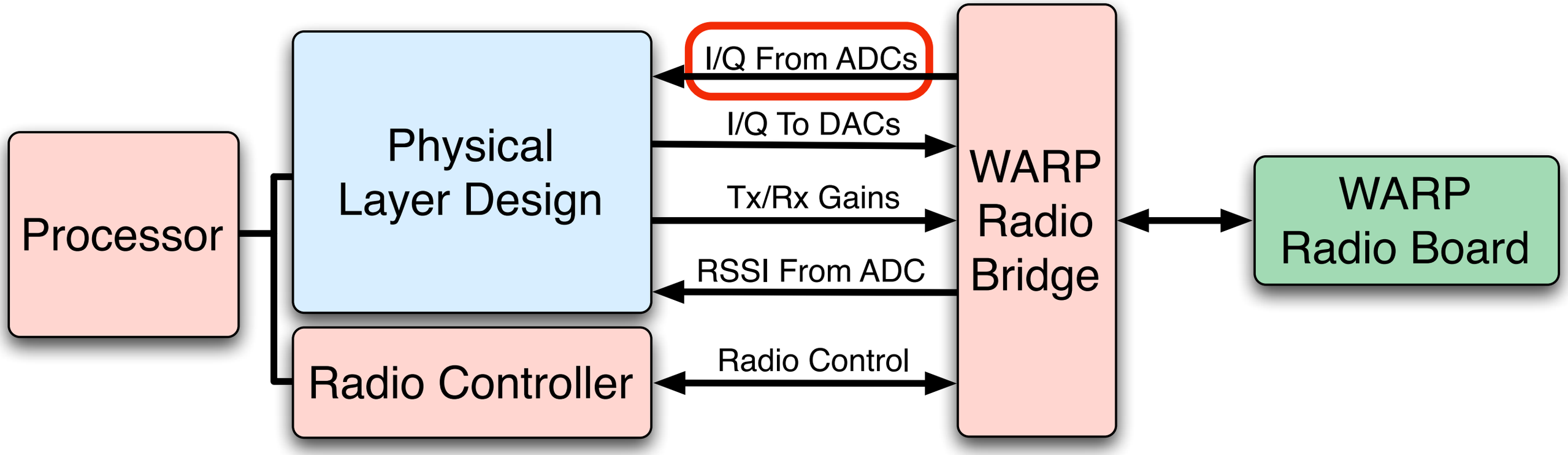


PHY-Radio Interface



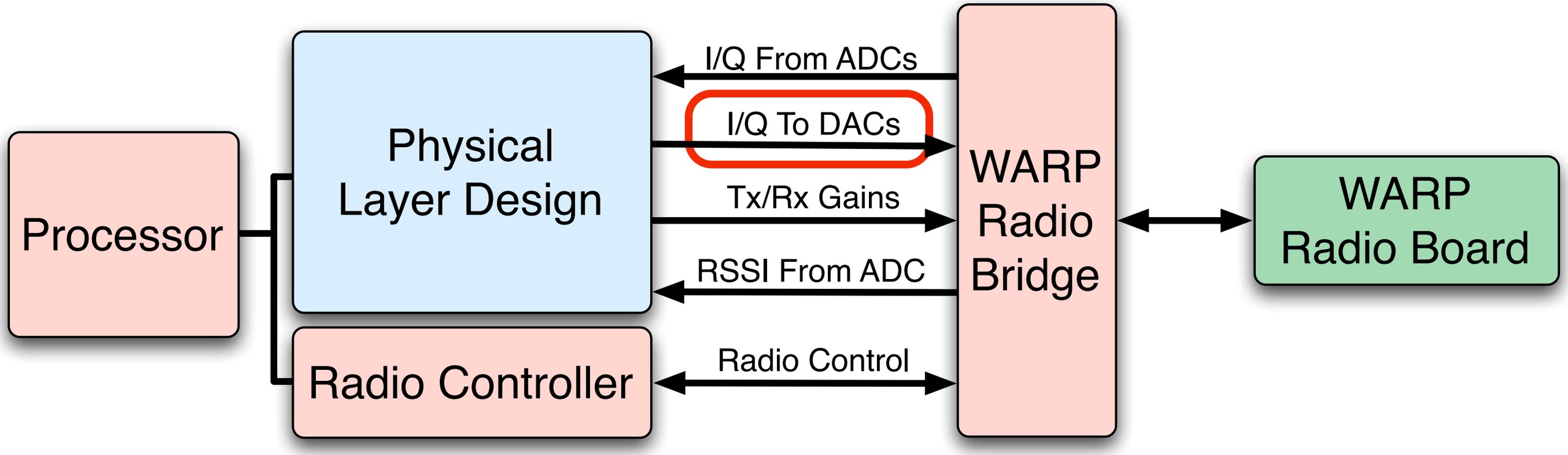
- Radio interface is real-time
- PHY/radio interface uses FPGA logic
- Many options for “information” source

PHY-Radio Interface



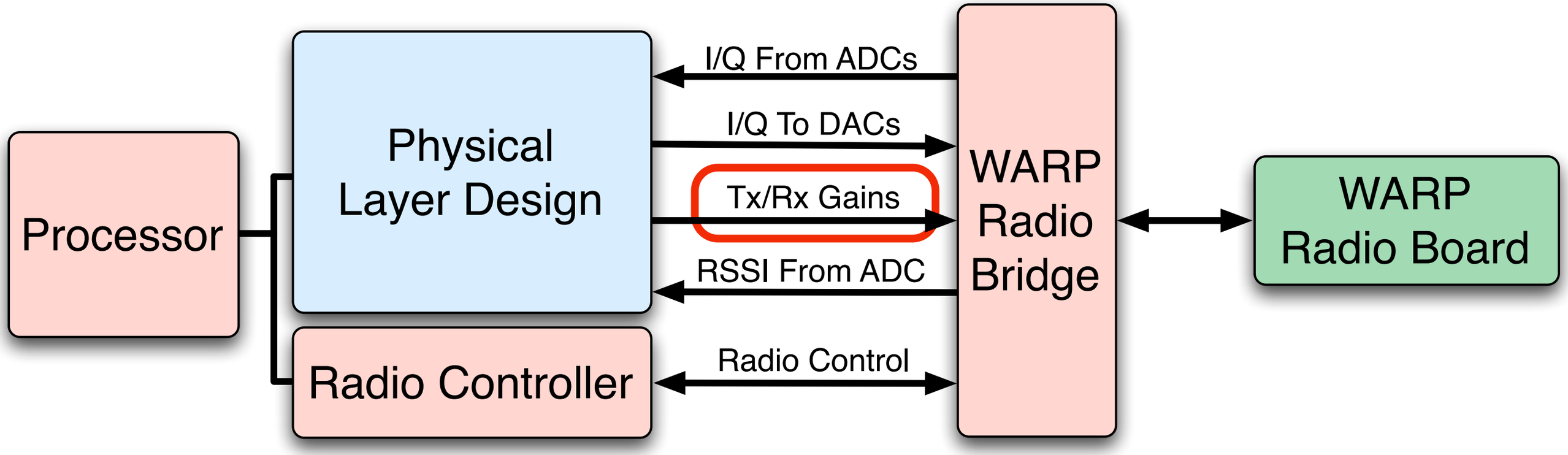
- Two 14-bit samples (I/Q) at 40MSps
- Direct sampling of radio I/Q outputs
- Radio settings are very important

PHY-Radio Interface



- Two 16-bit samples (I/Q) at 40MSps
- Direct sampling to radio I/Q inputs

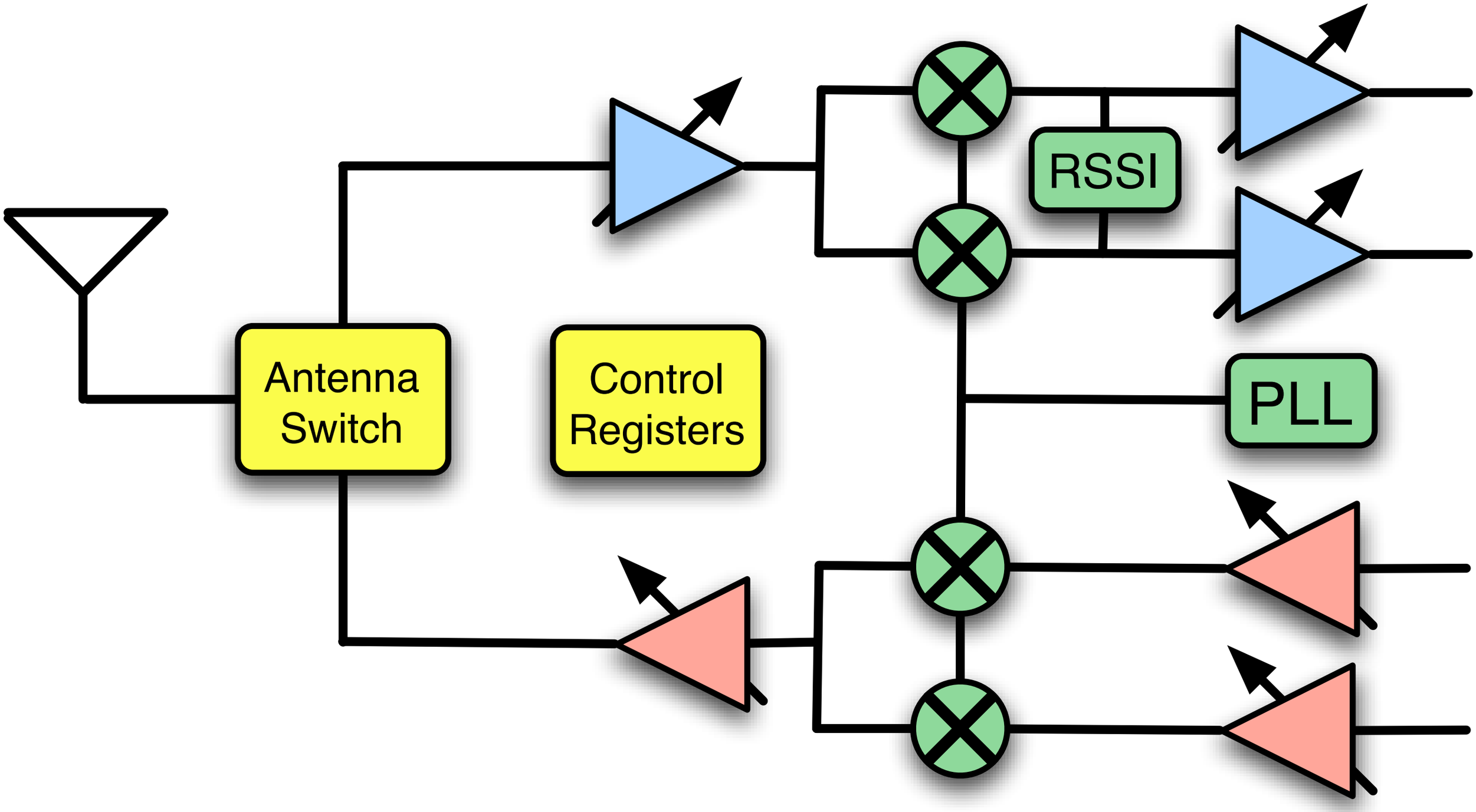
PHY-Radio Interface



- Four variable-gain amplifiers in Tx/Rx paths
- All under FPGA control

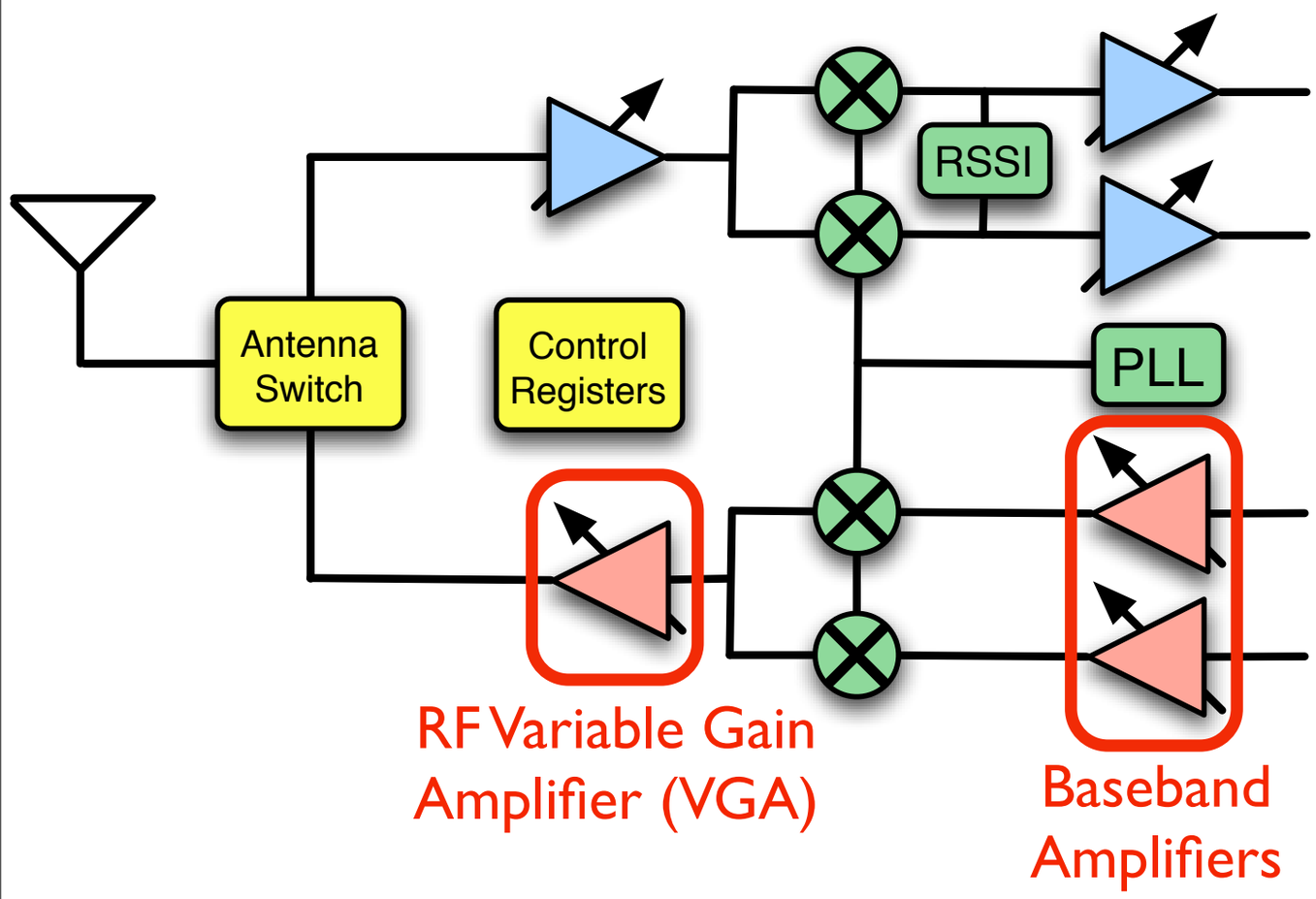
PHY-Radio Interface

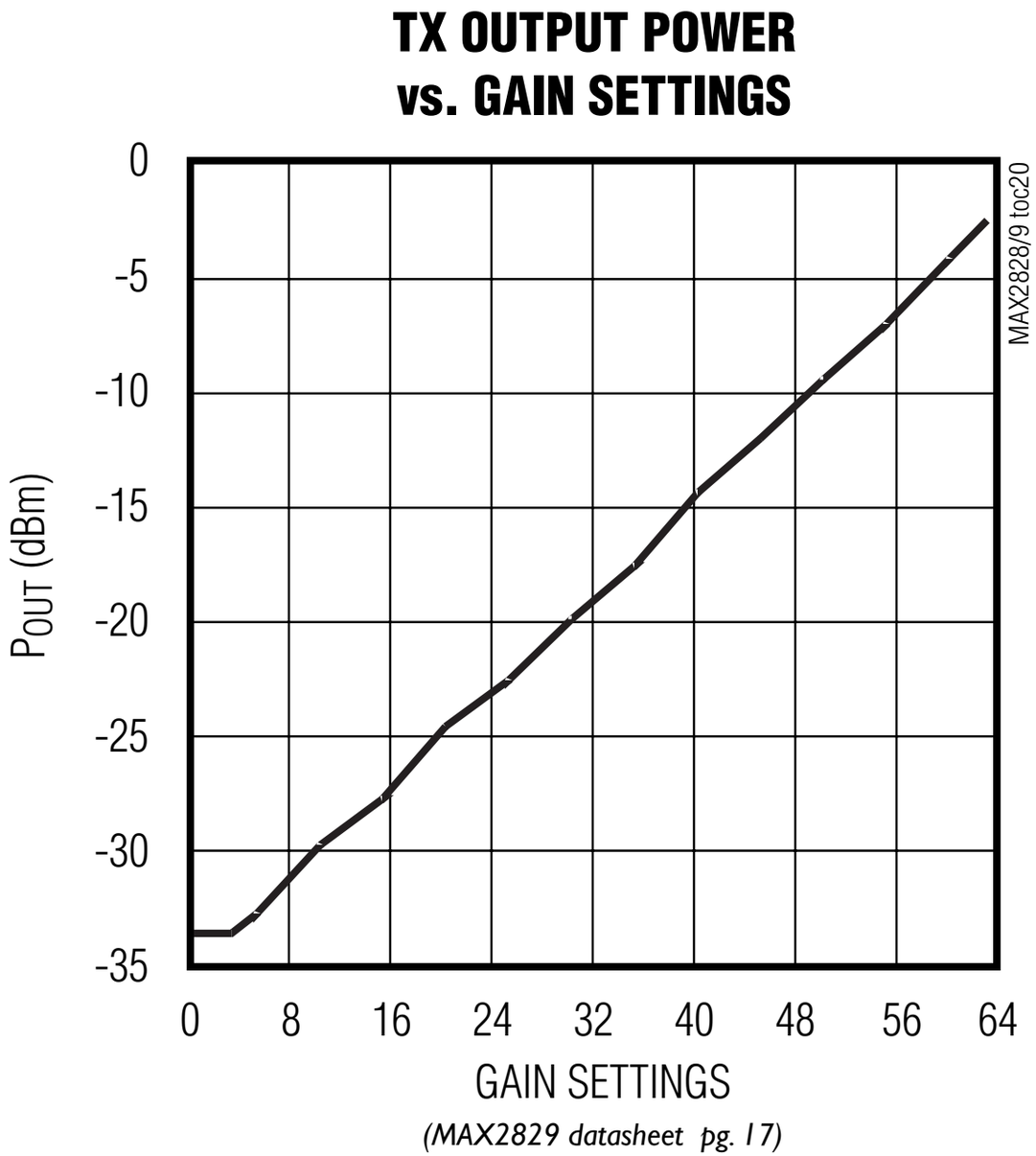
Radio Block Diagram



PHY-Radio Interface

Tx Gains

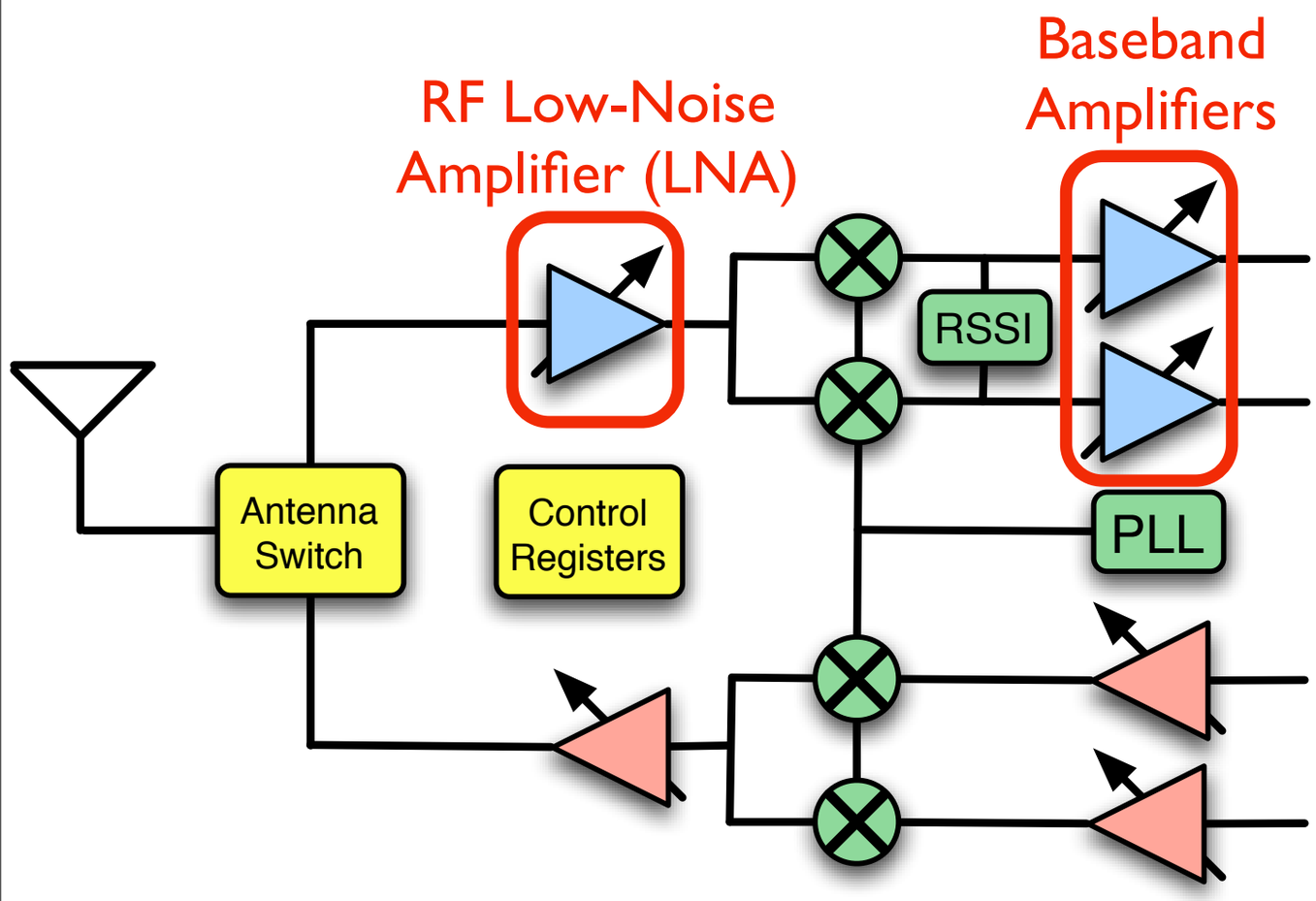


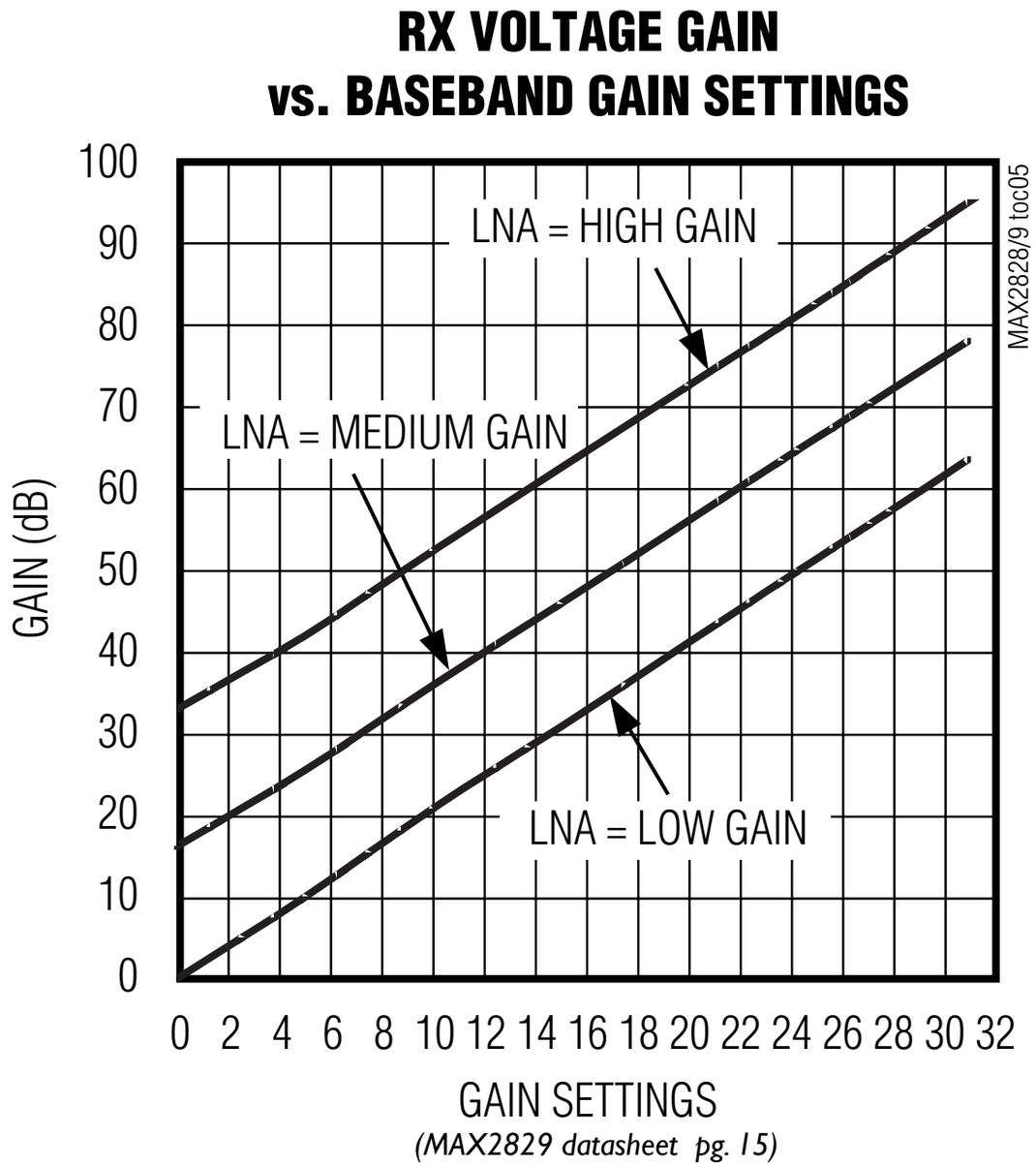


(MAX2829 datasheet pg. 17)

PHY-Radio Interface

Rx Gains

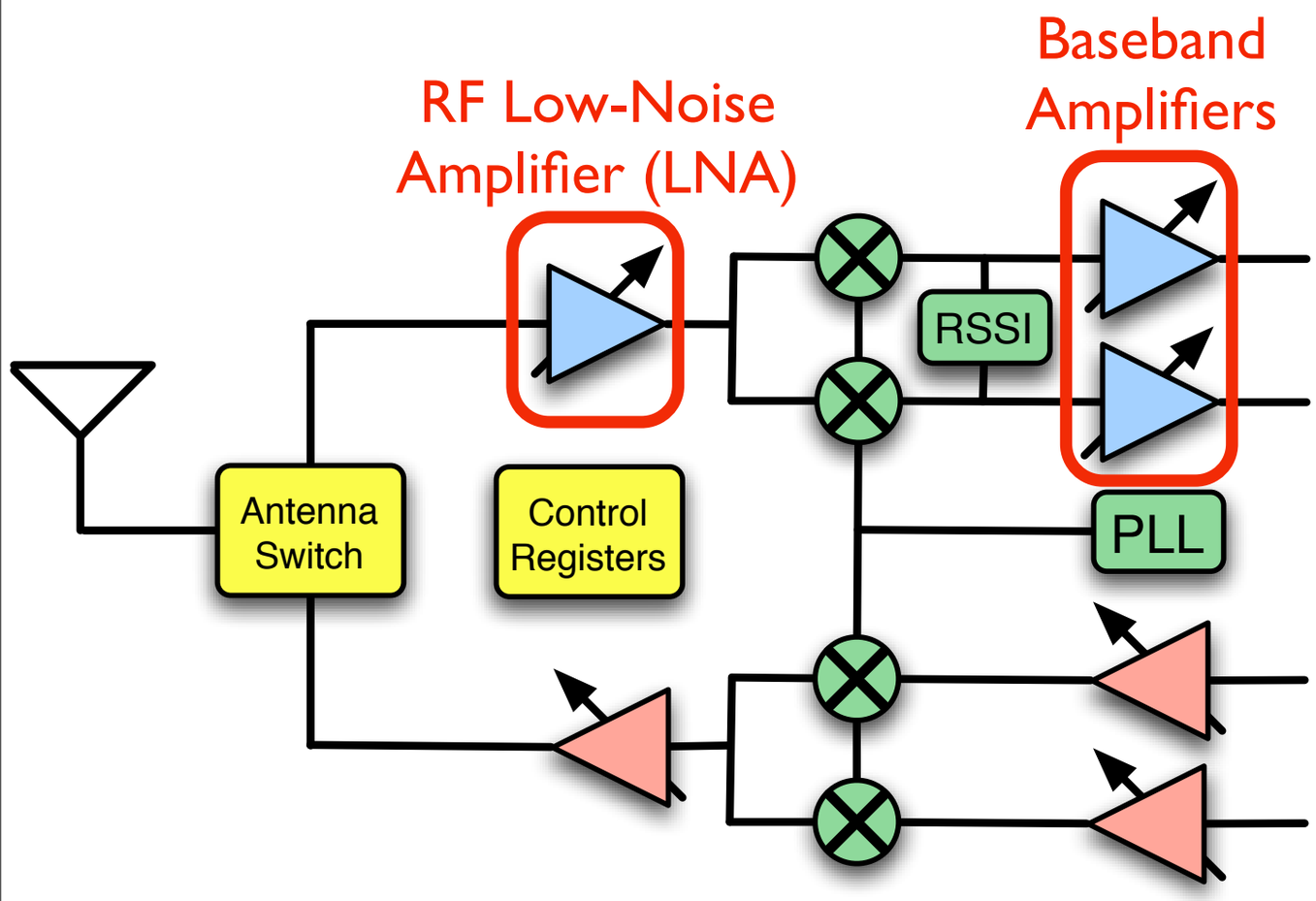


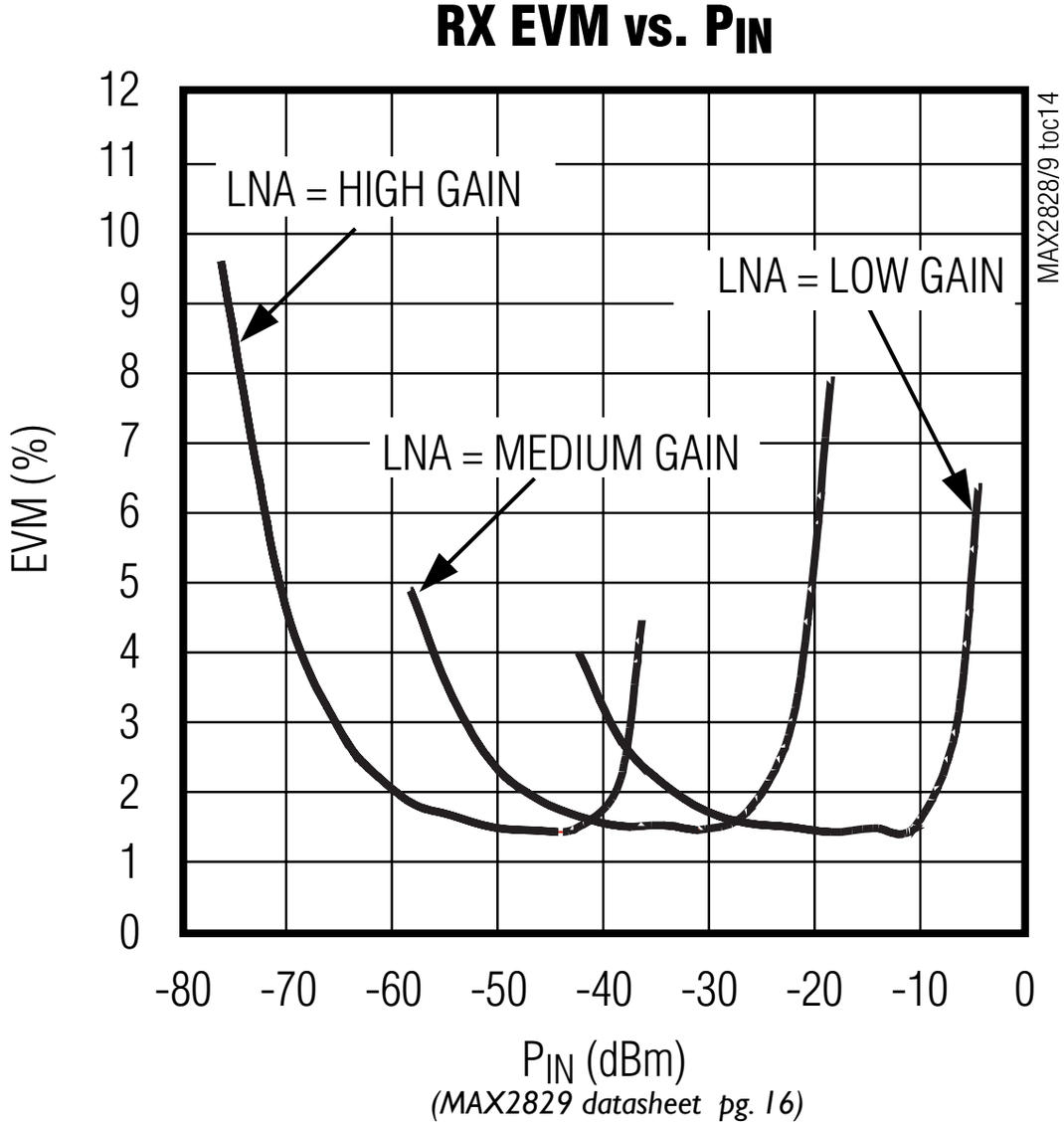


(MAX2829 datasheet pg. 15)

PHY-Radio Interface

Rx Gains

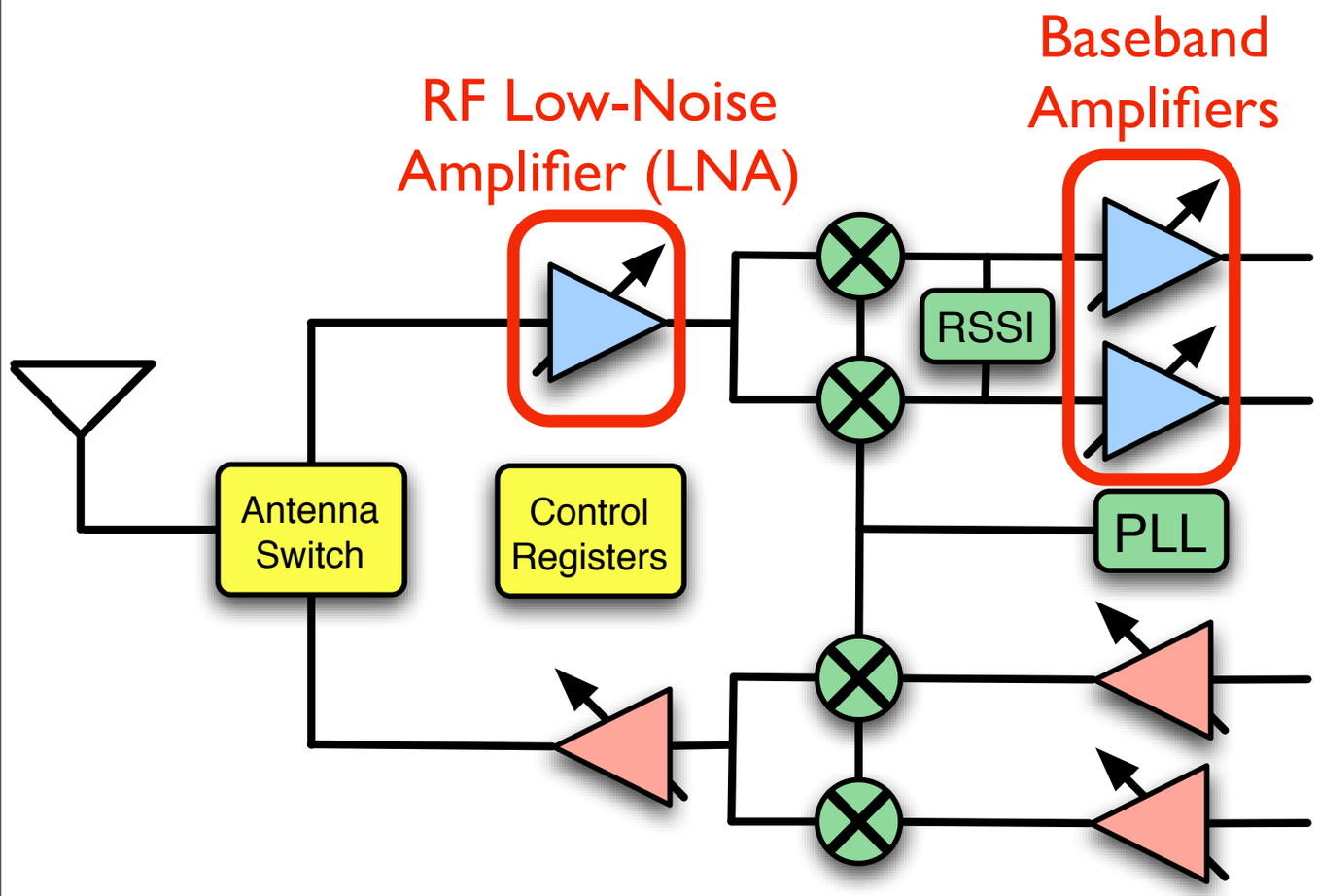


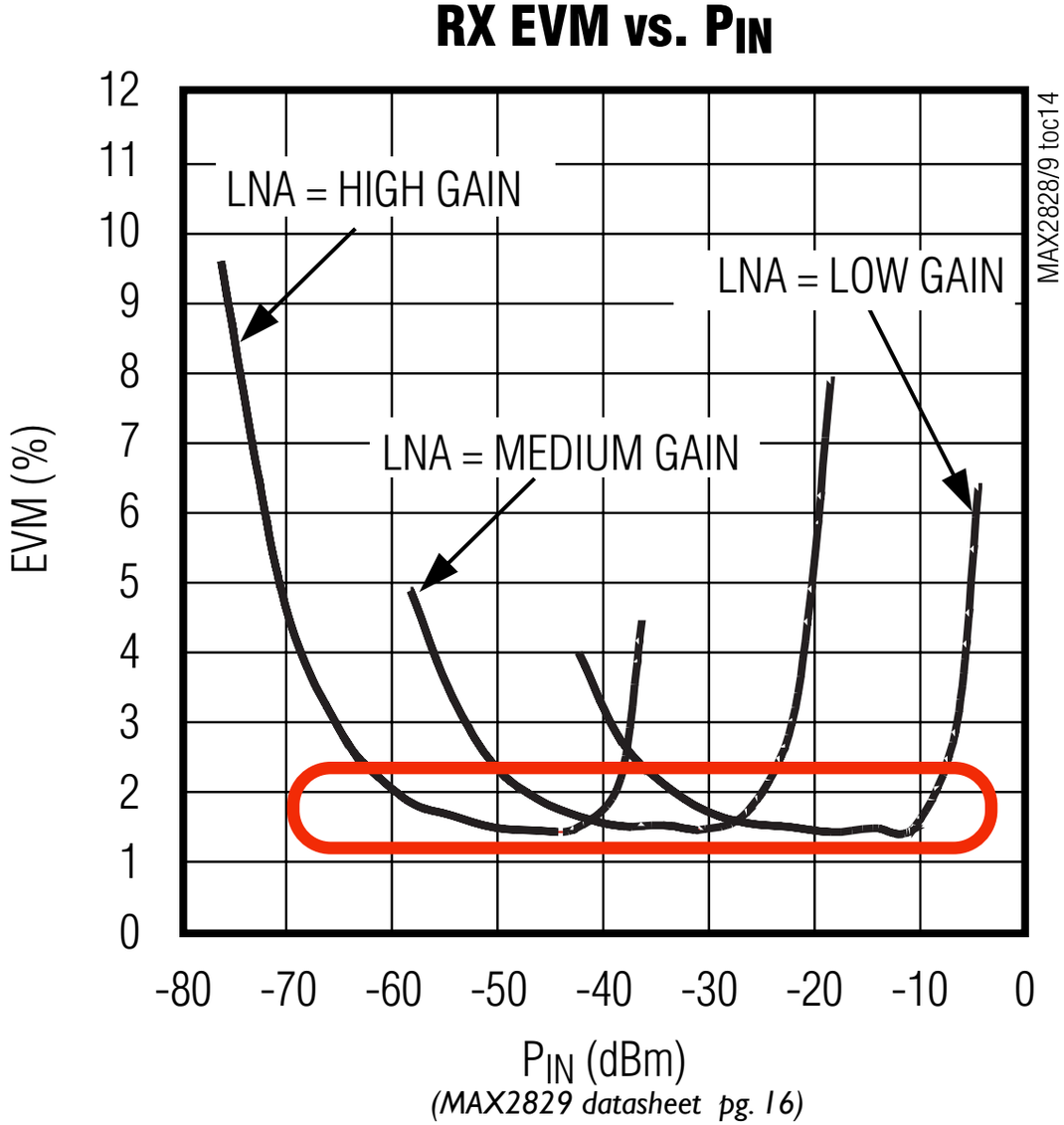


(MAX2829 datasheet pg. 16)

PHY-Radio Interface

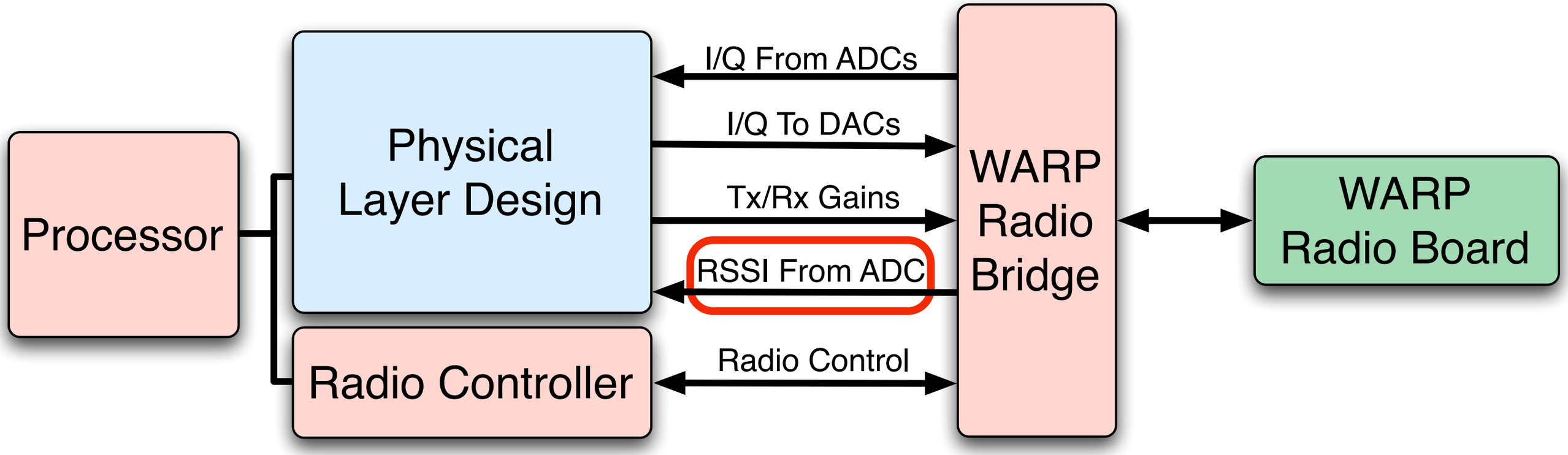
Rx Gains





(MAX2829 datasheet pg. 16)

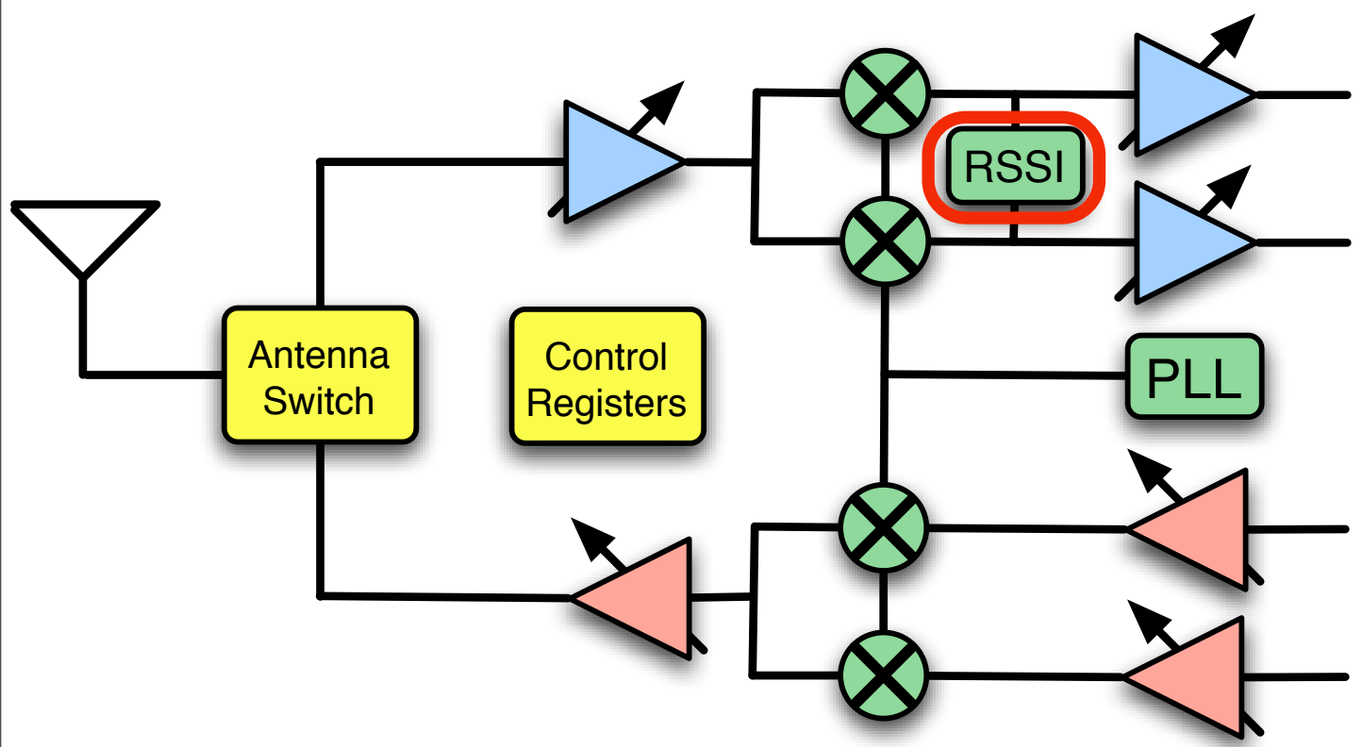
PHY-Radio Interface

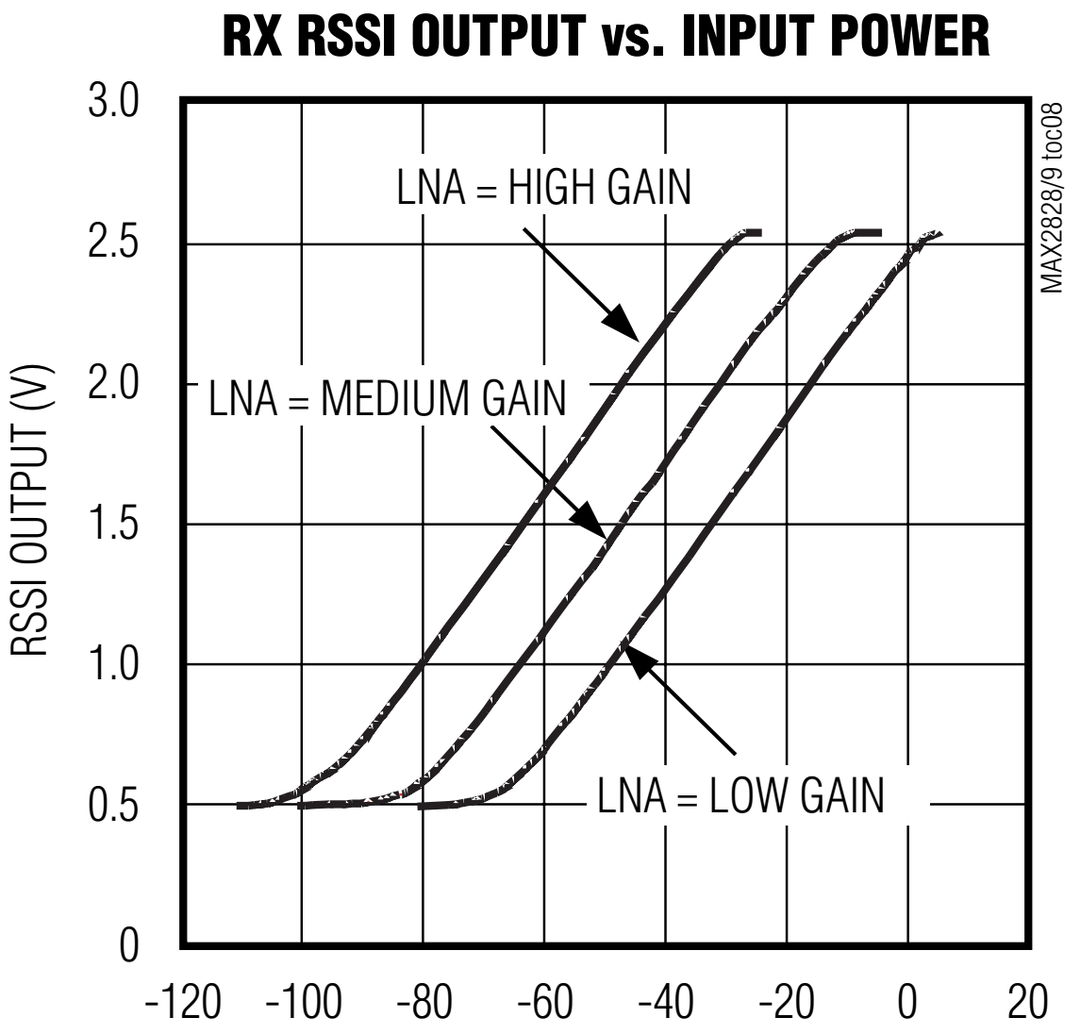


- 10-bit samples at 10Msps
- Direct sampling of radio's RSSI output

PHY-Radio Interface

RSSI

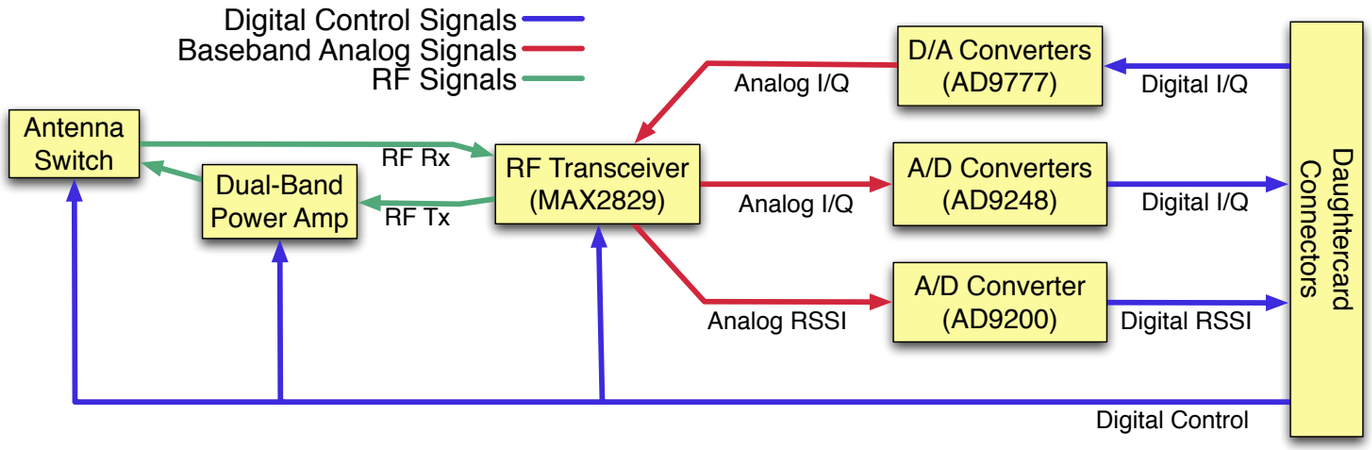


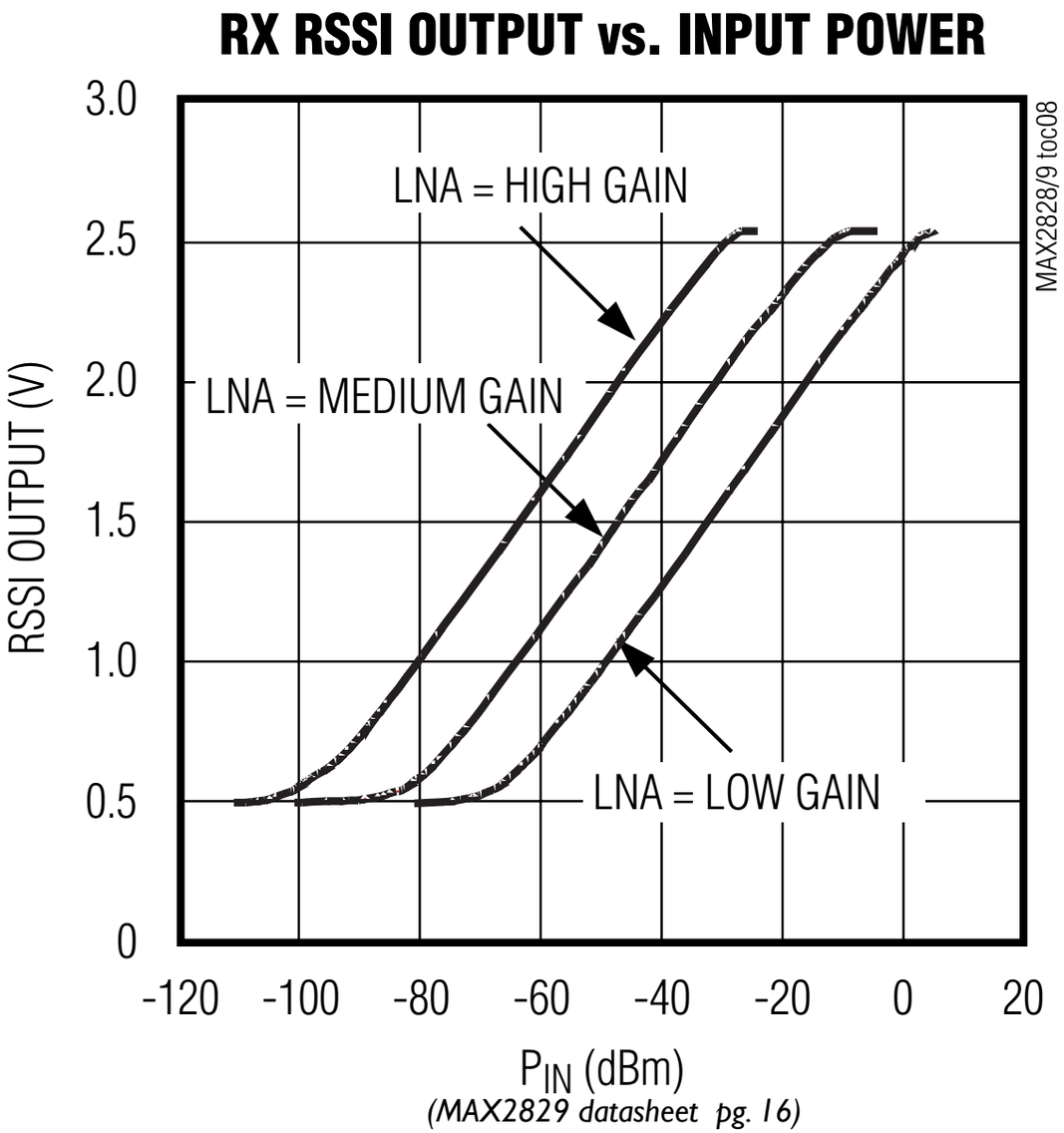


(MAX2829 datasheet pg. 16)

PHY-Radio Interface

RSSI

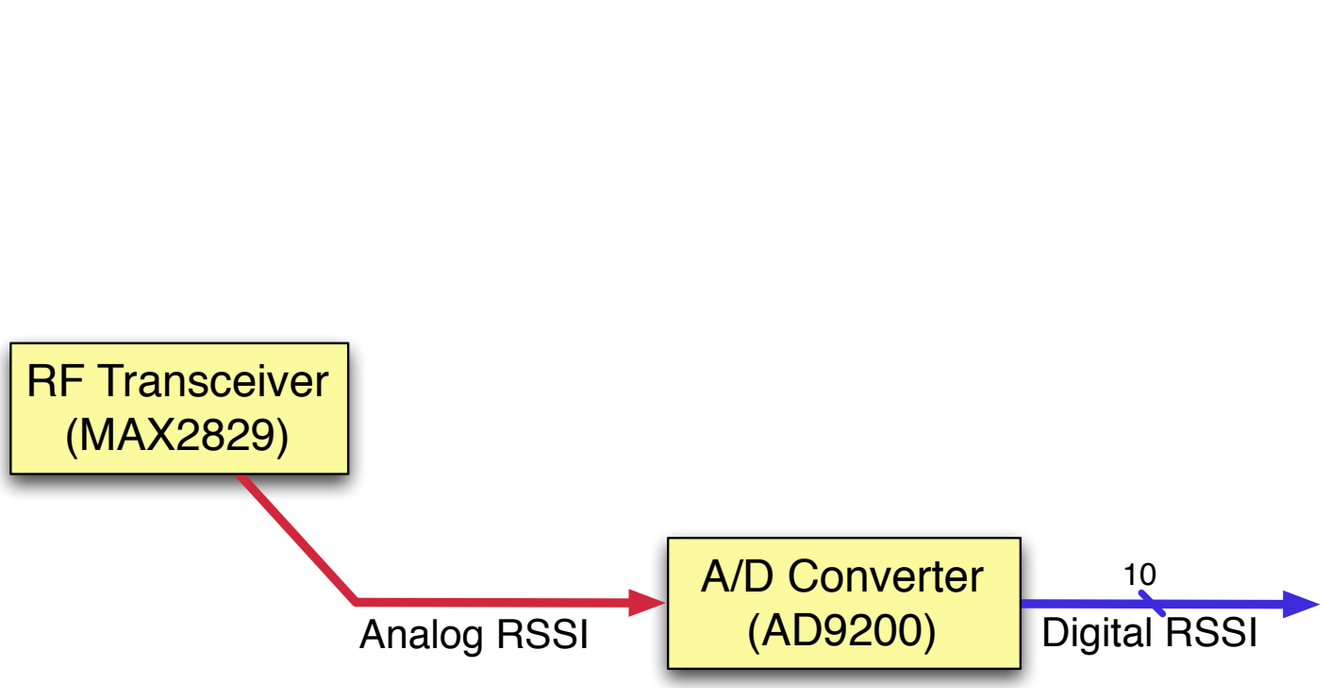




(MAX2829 datasheet pg. 16)

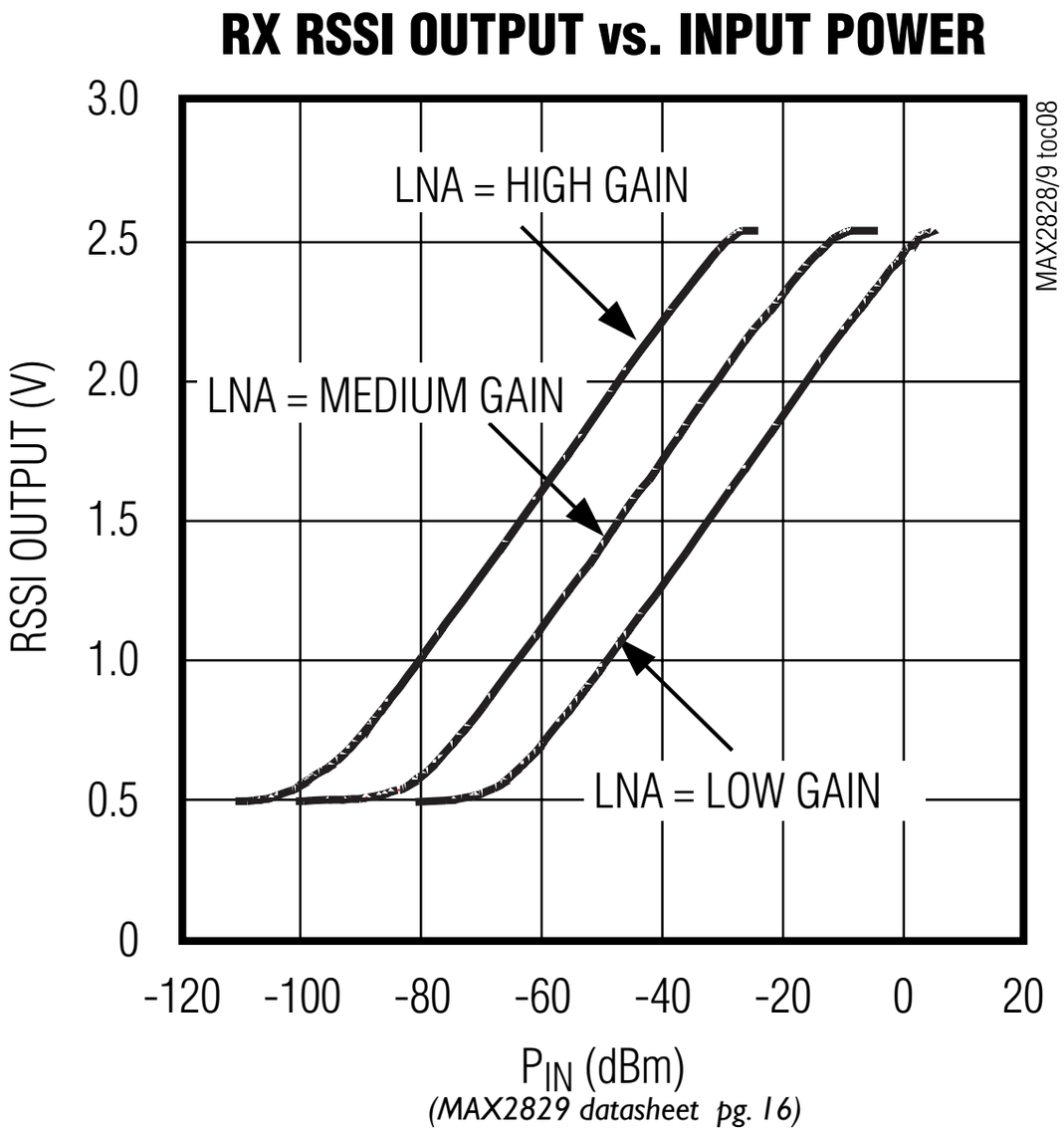
PHY-Radio Interface

RSSI



0.5v ⇒ RSSI_ADC[9:0] = 0

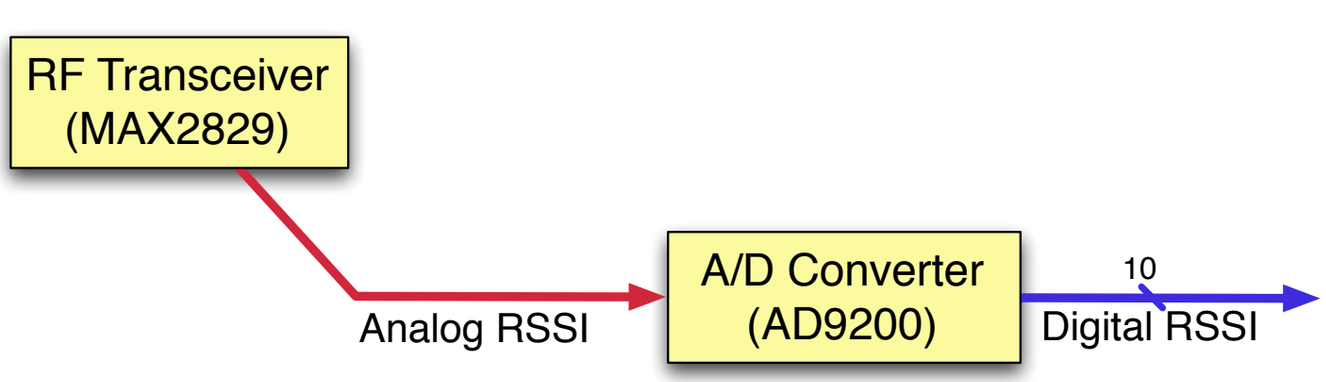
2.5v ⇒ RSSI_ADC[9:0] = 1023



(MAX2829 datasheet pg. 16)

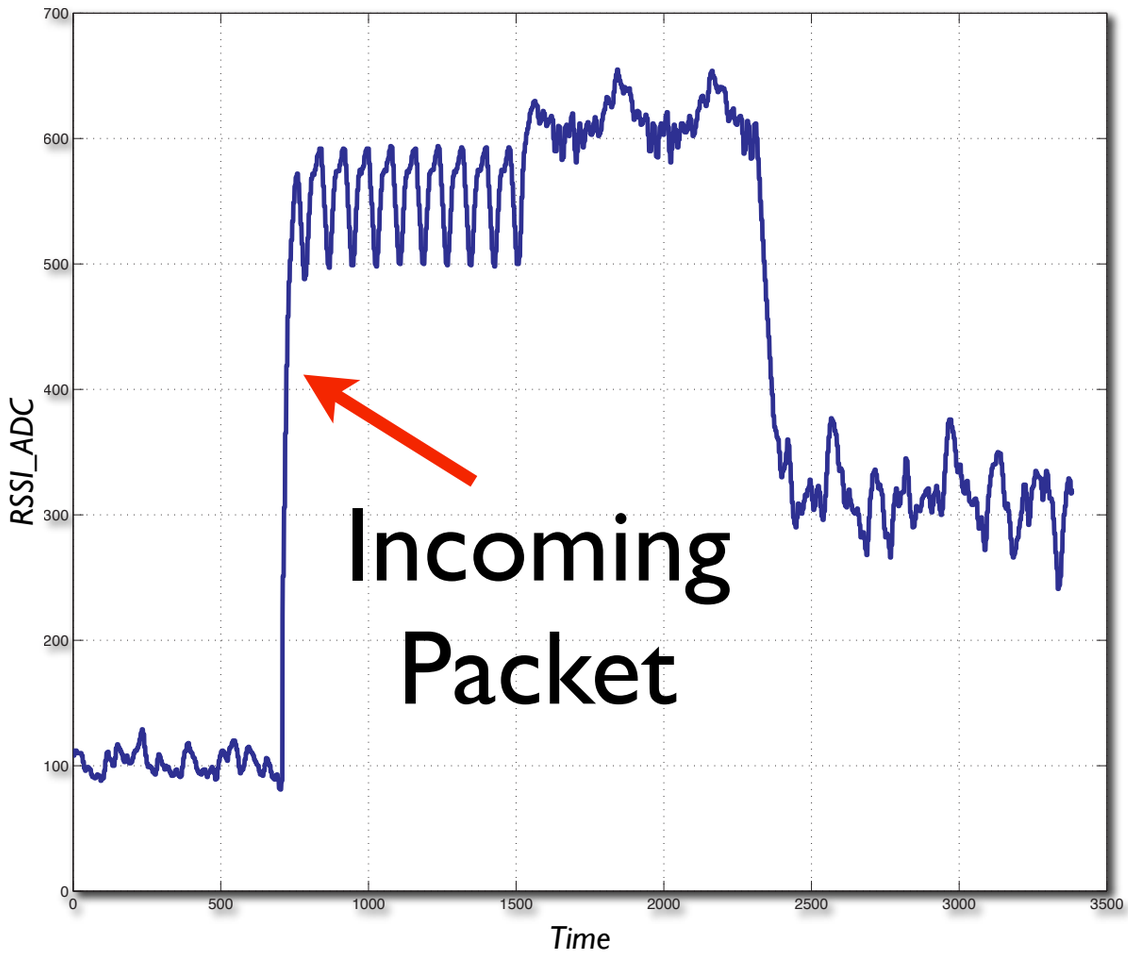
PHY-Radio Interface

RSSI

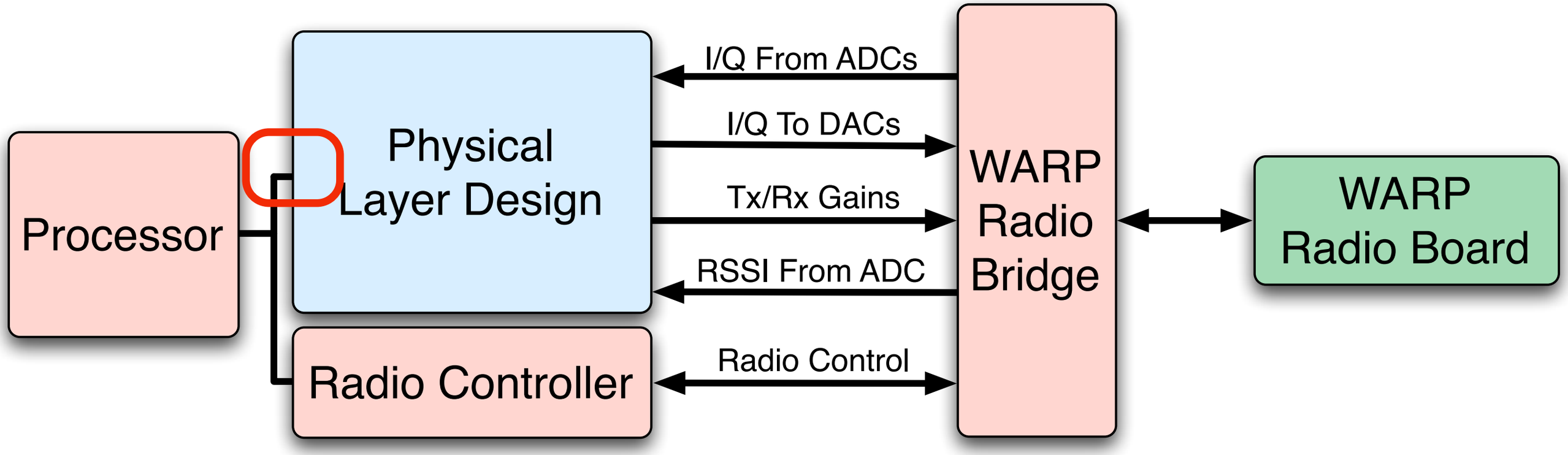


0.5v ⇒ RSSI_ADC[9:0] = 0

2.5v ⇒ RSSI_ADC[9:0] = 1023



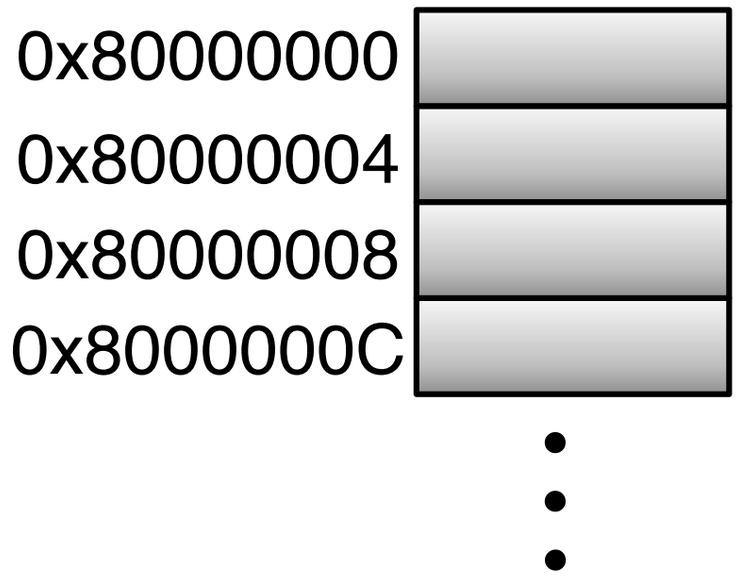
PHY-Processor Interface



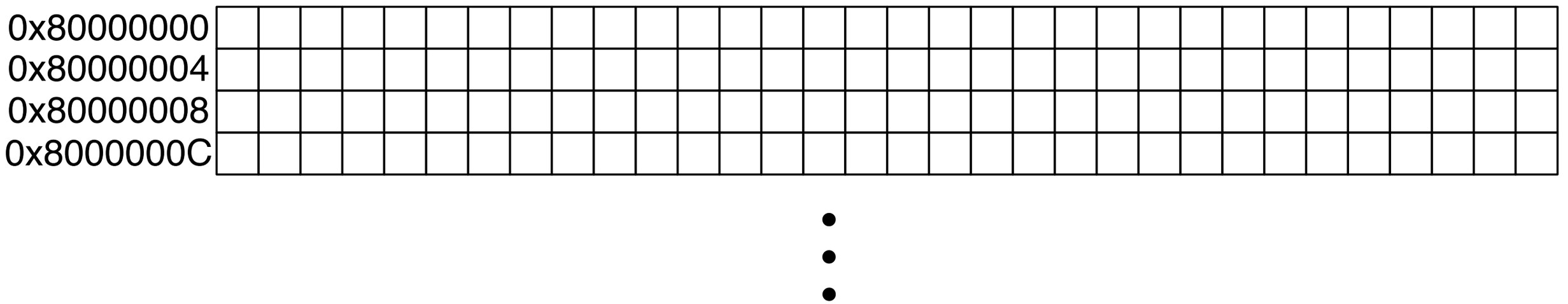
- PHY is a memory mapped peripheral
- Uses both registers and memory blocks
- Bus interface is generated automatically

PHY-Processor Interface

Software sees 32-bit memory space

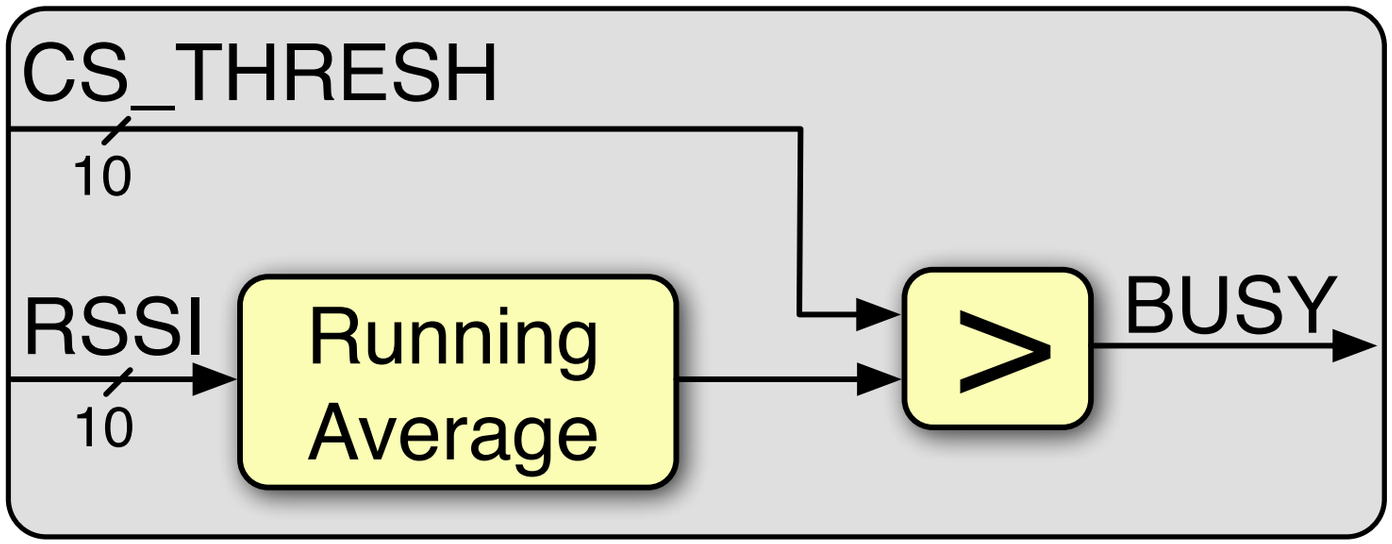


Hardware sees 32 wires per address



PHY-Processor Interface

Example

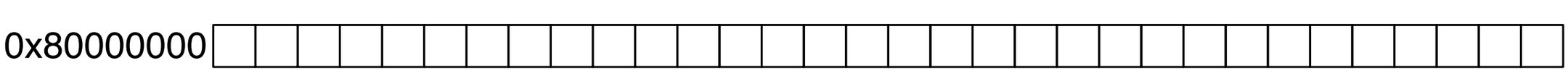


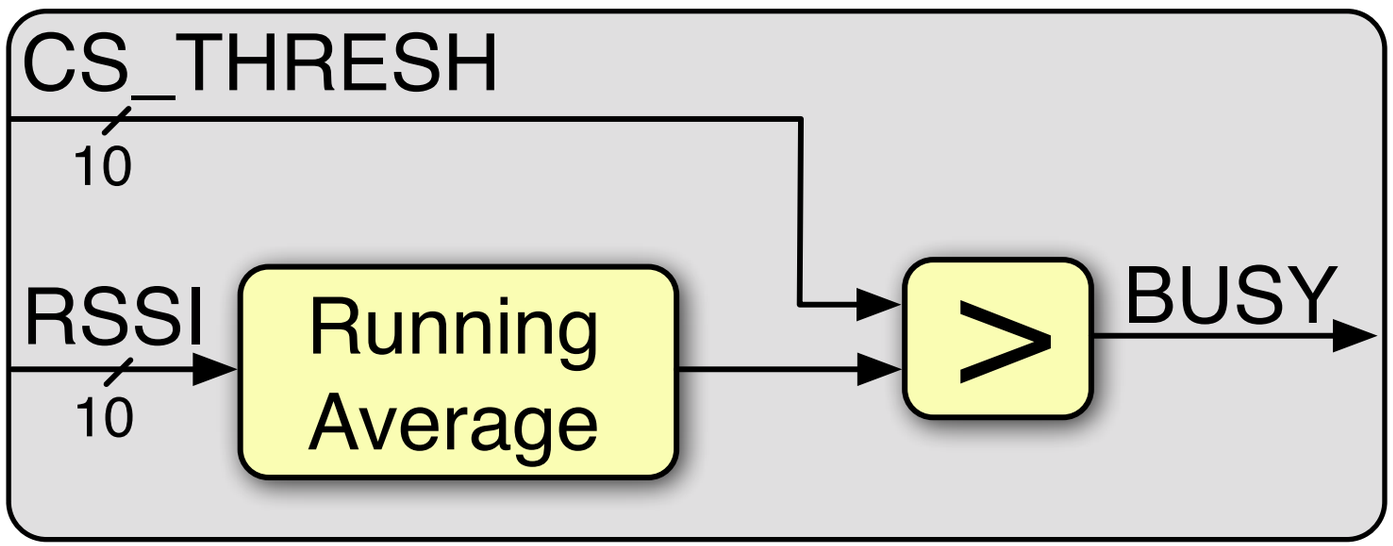
Carrier Sensing Logic

PHY-Processor Interface

Example

PHY uses memory-mapped wires for:





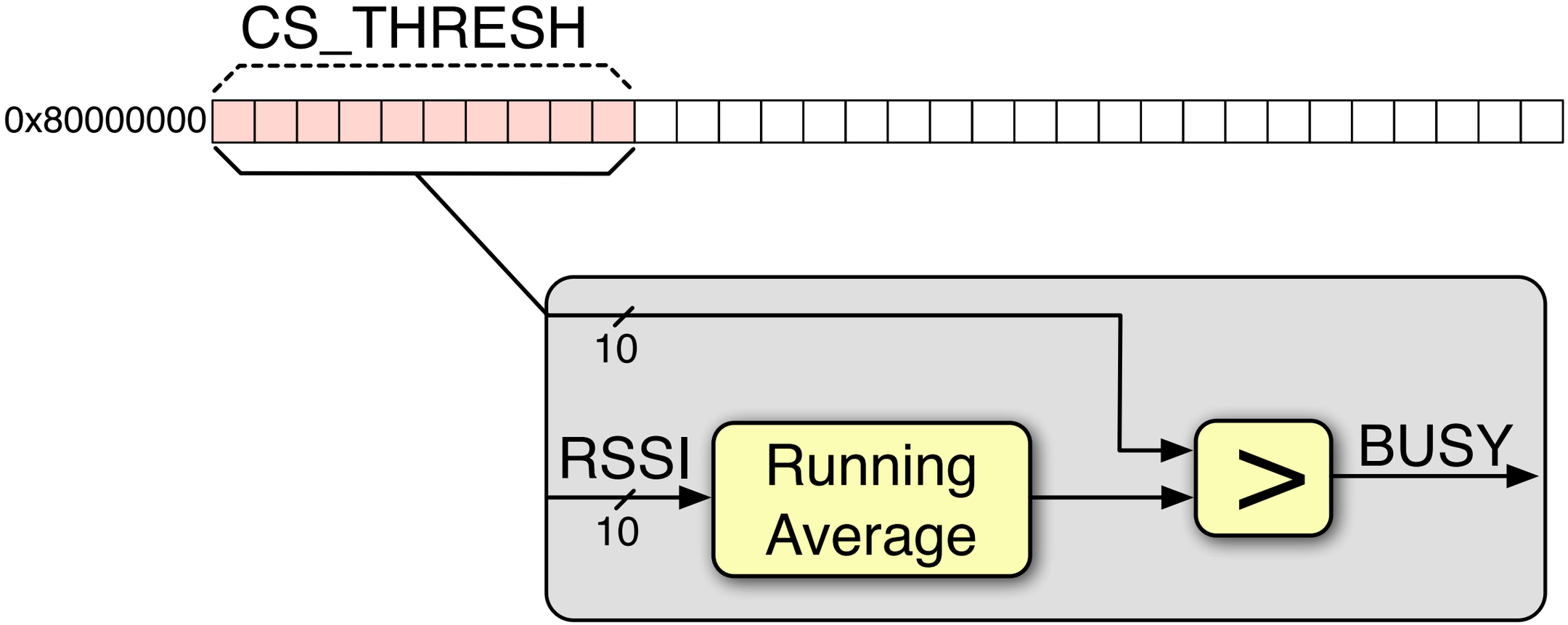
Carrier Sensing Logic

PHY-Processor Interface

Example

PHY uses memory-mapped wires for:

- Parameters



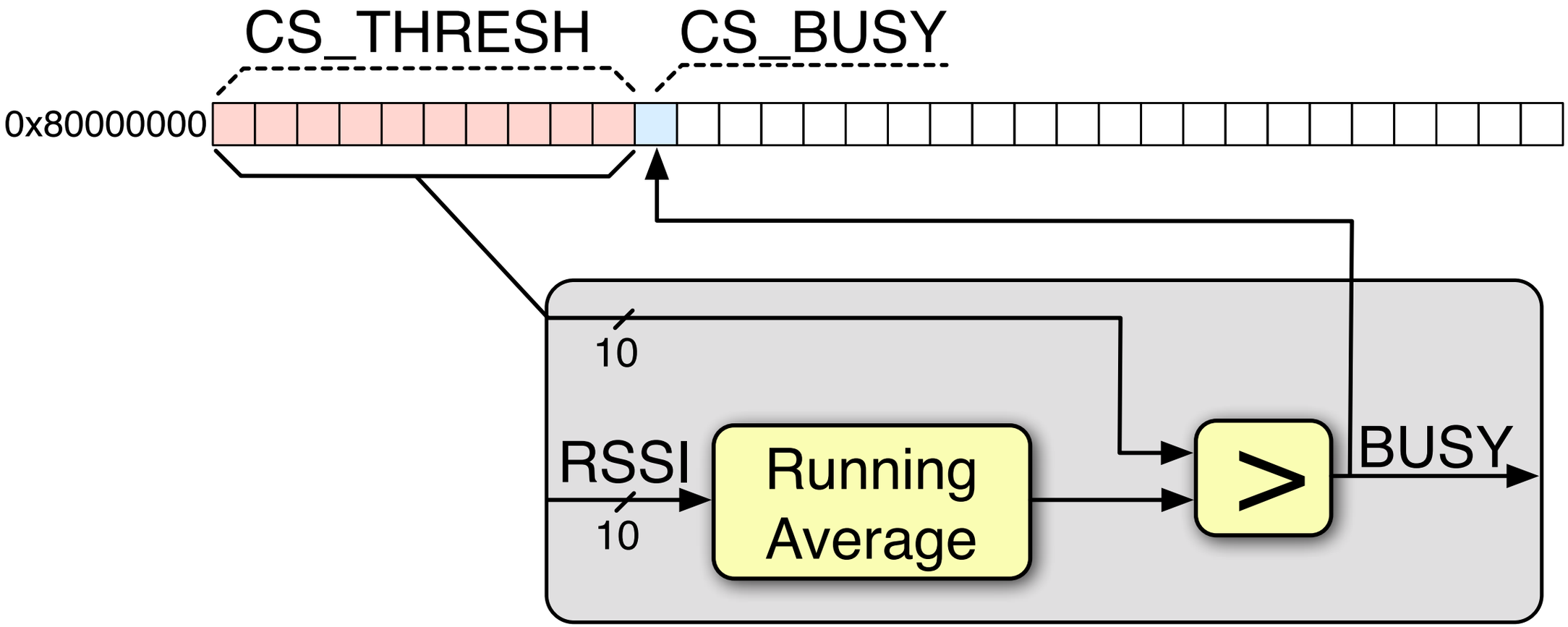
Carrier Sensing Logic

PHY-Processor Interface

Example

PHY uses memory-mapped wires for:

- Parameters
- Feedback



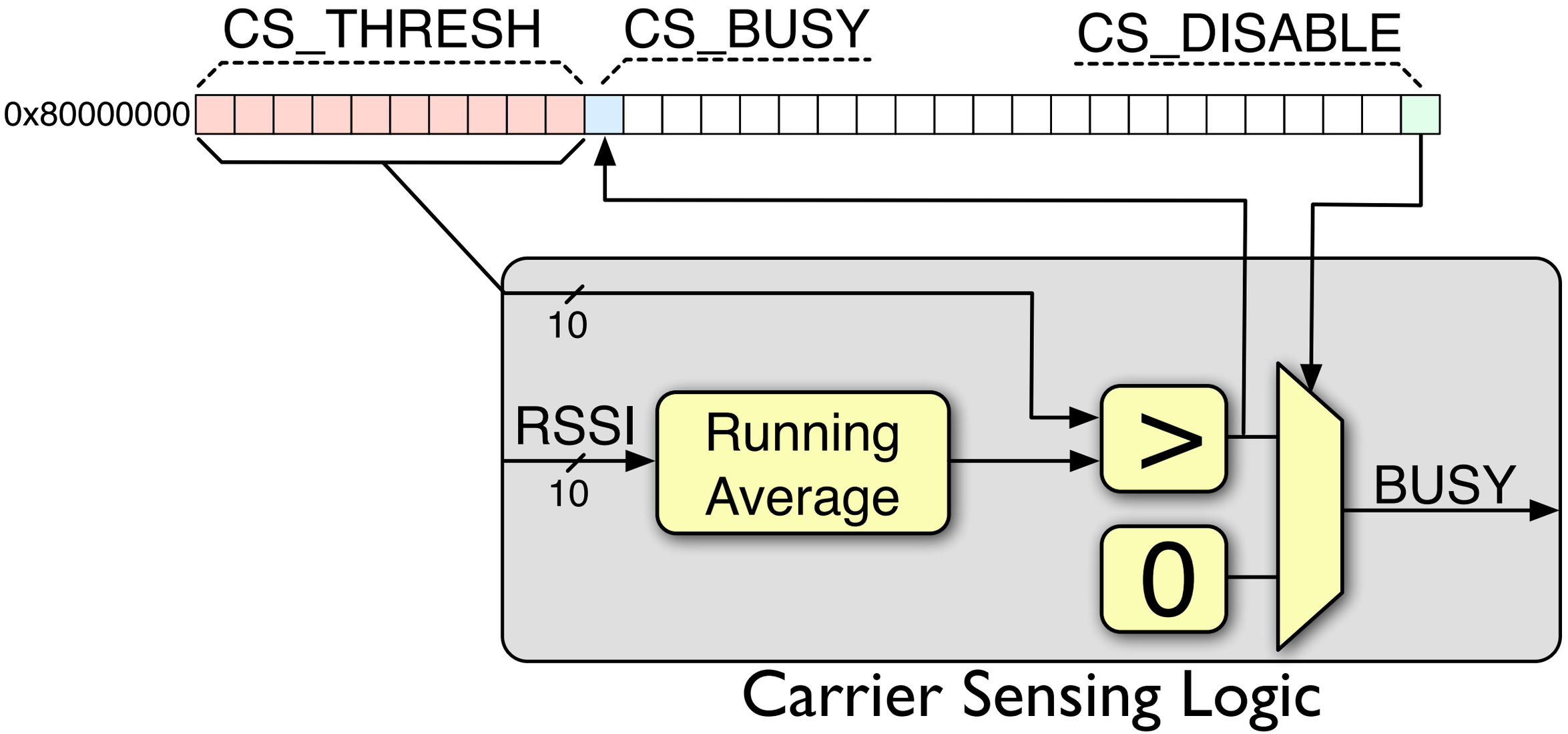
Carrier Sensing Logic

PHY-Processor Interface

Example

PHY uses memory-mapped wires for:

- Parameters
- Feedback
- Control



Carrier Sensing Logic

PHY-Processor Interface

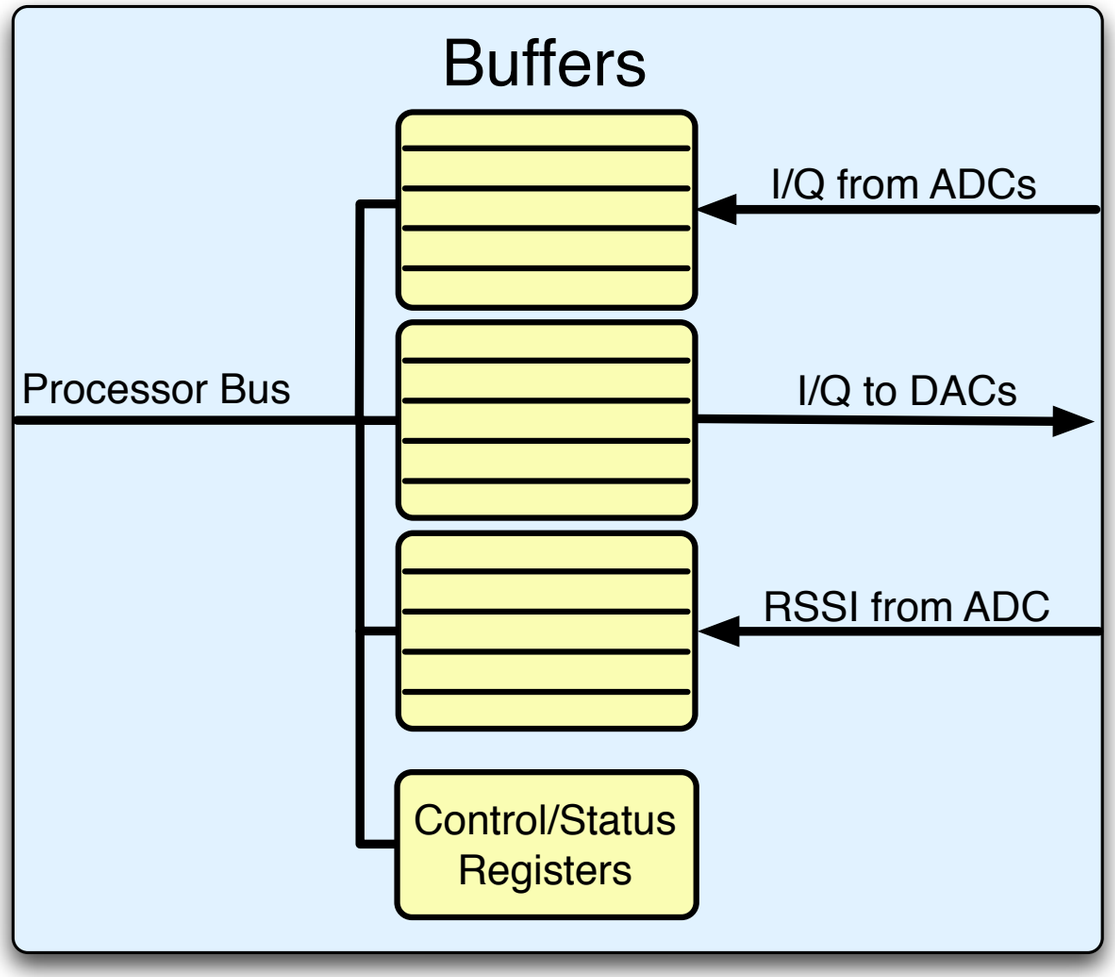
- Hardware/software ≠ PHY/MAC
  - Some MAC functions in logic
  - Some PHY control in software
- Parameterization vs. complexity is tradeoff
  - Easier to iterate on software
  - Designing flexible hardware is tricky

Transceiver Examples

- WARPLab
- MIMO OFDM

Transceiver Examples

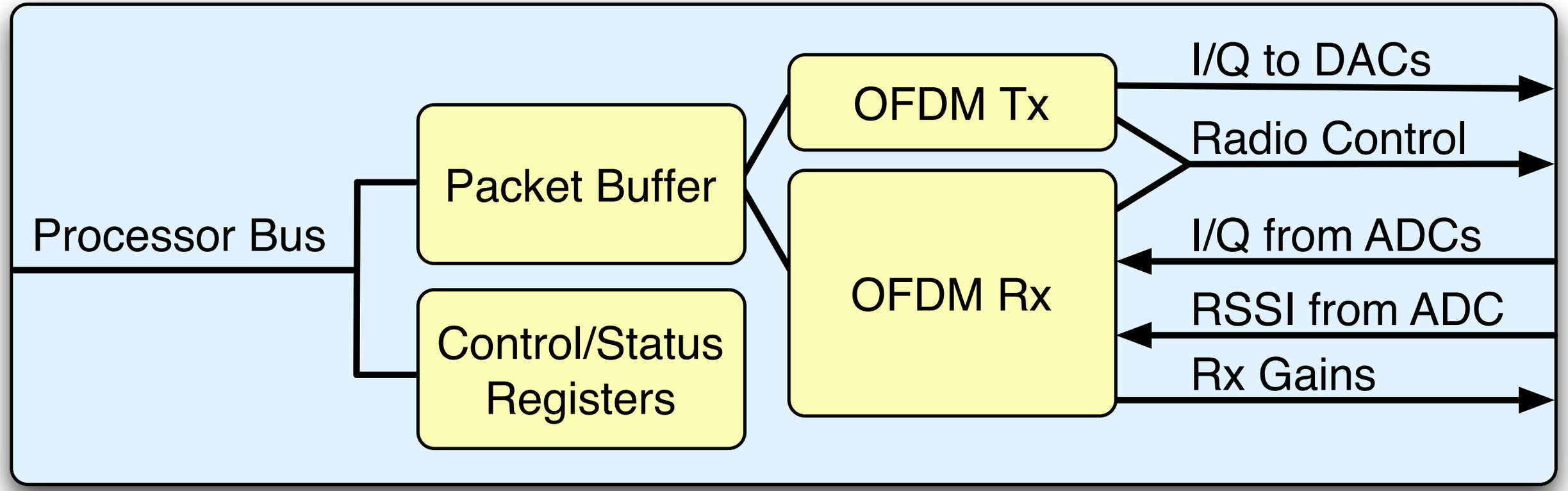
WARPLab Transceiver



- Application provides digital waveforms
- Transceiver handles radio data I/O
- Software handles radio control

Transceiver Examples

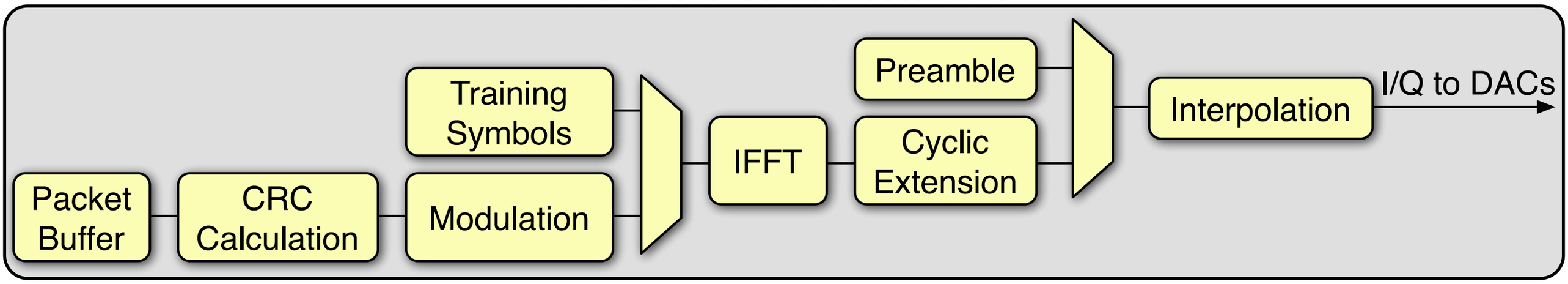
OFDM Transceiver



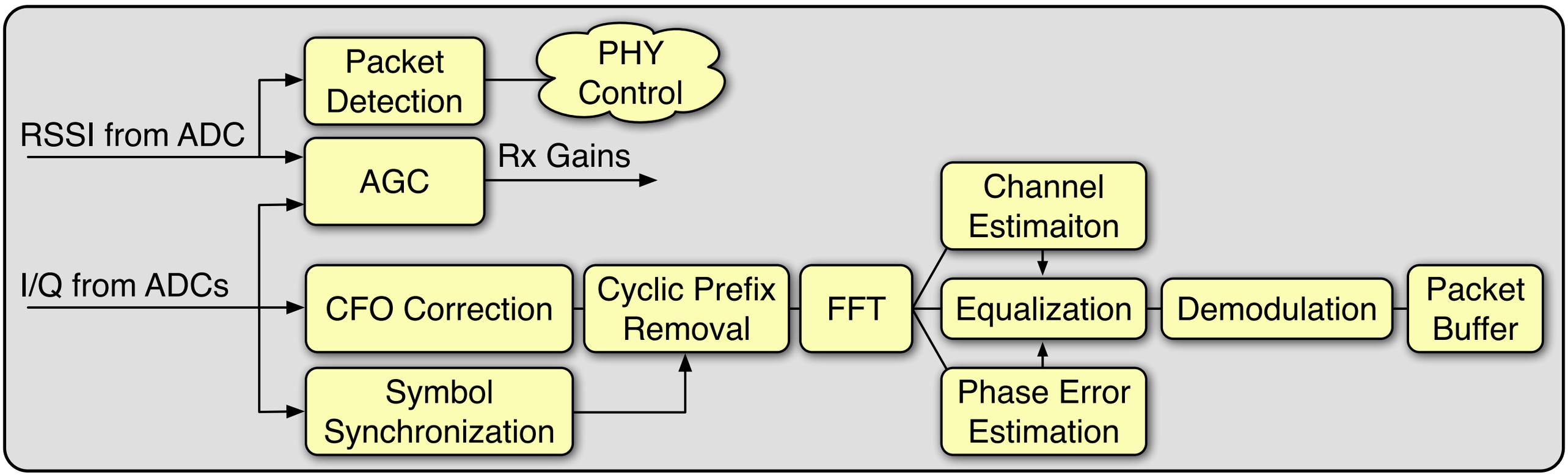
- Application provides packets & parameters
- PHY processes waveforms and radio I/O
- All processing is real-time

Transceiver Examples

OFDM Transmitter



OFDM Receiver



Questions?

(Lab 3 is next)

Lab 3: Simple Transceiver

- Build a simple transmitter in Sysgen
- Convert the model to a PLB peripheral
- Connect the Tx core to the radio bridge
- Test the model at RF
- Add an RSSI-based receiver
- Update the hardware and test