WARP: Physical Layer Design

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WARP Workshop
Rice University
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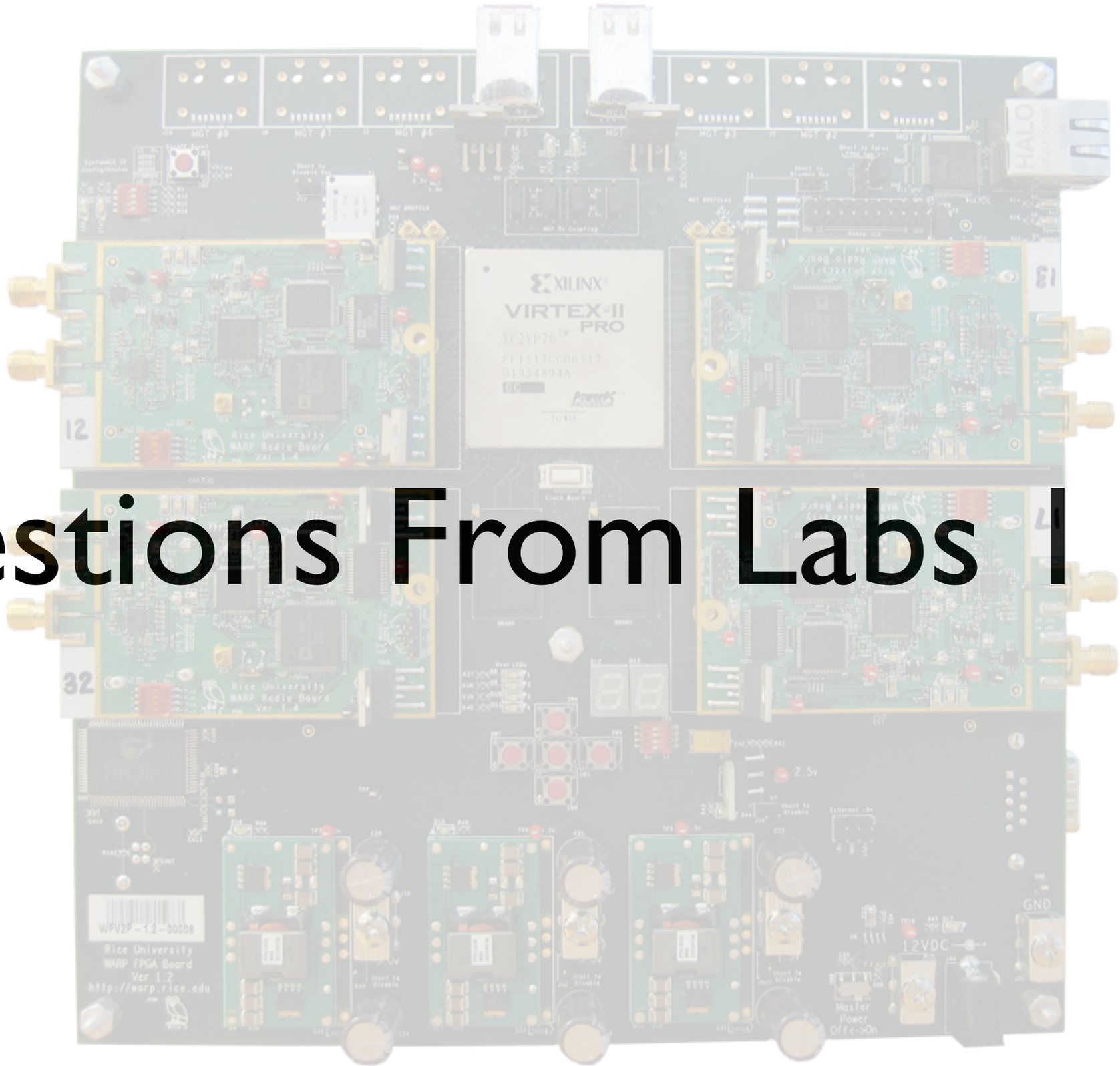
warp.rice.edu

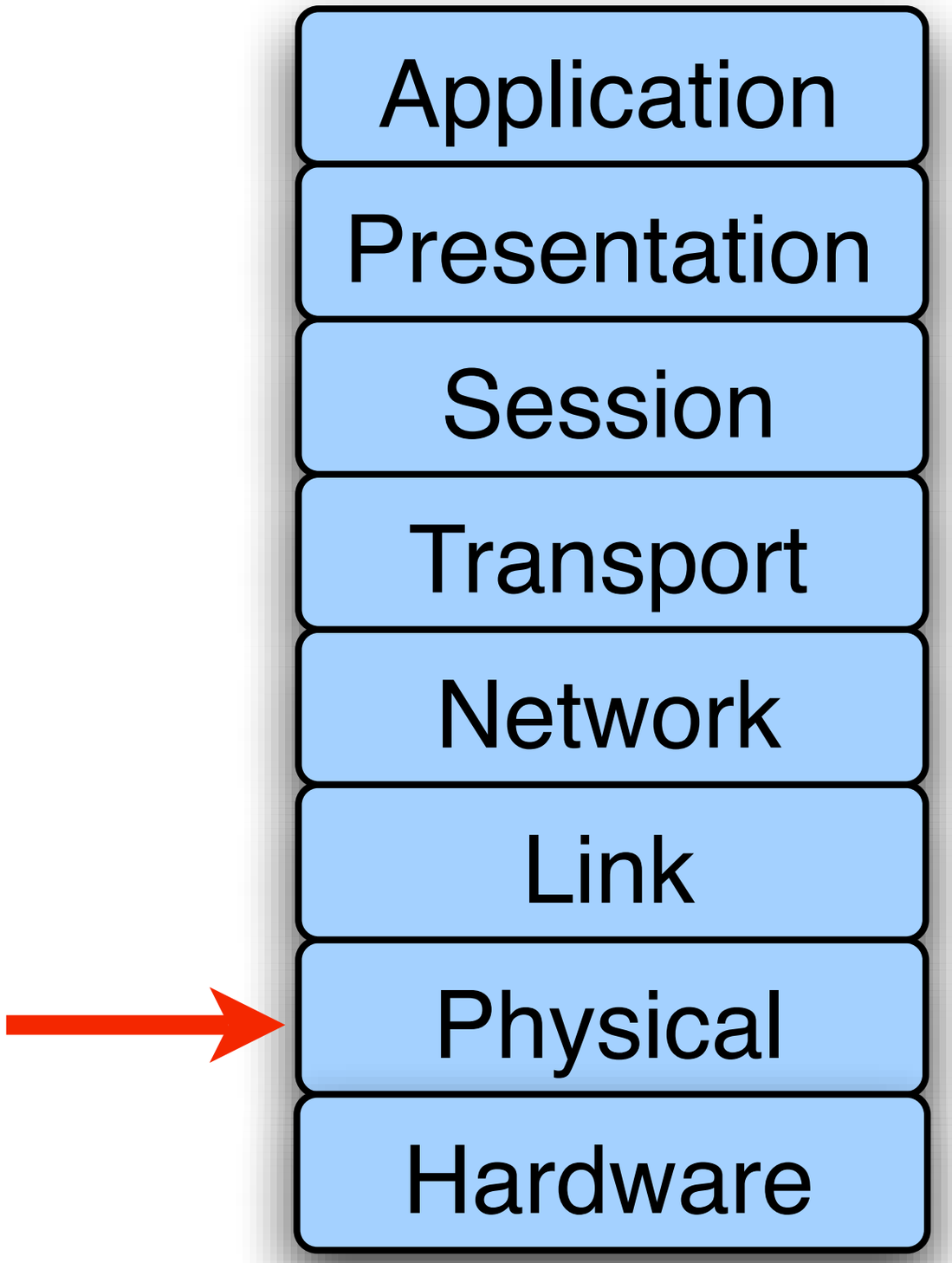
Questions From Labs 1 & 2?



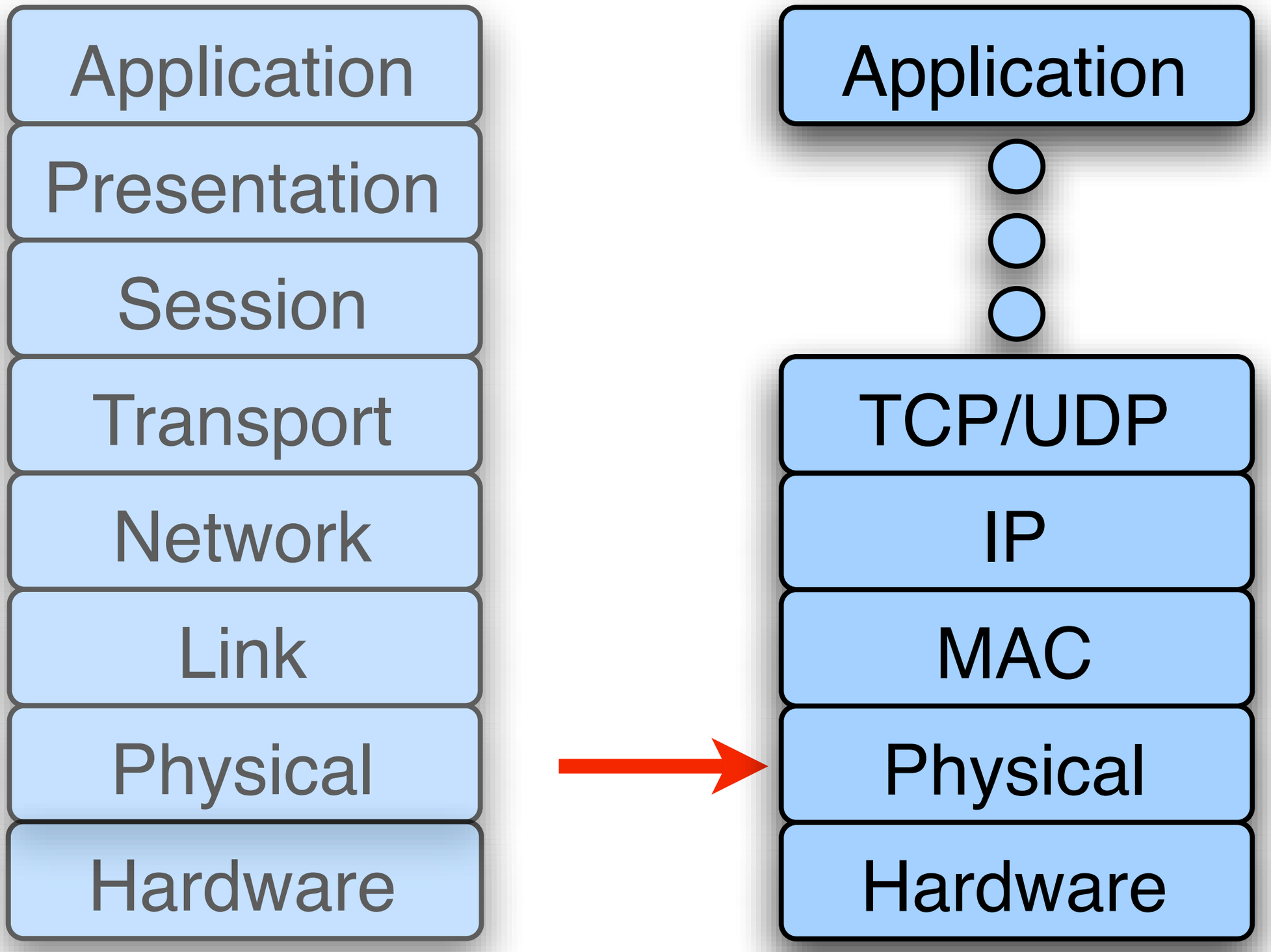
PHY Design - Outline

- Physical Layer Basics
- Real-time Physical Layer Design Flow
- Lab 3: Building a Simple Transmitter

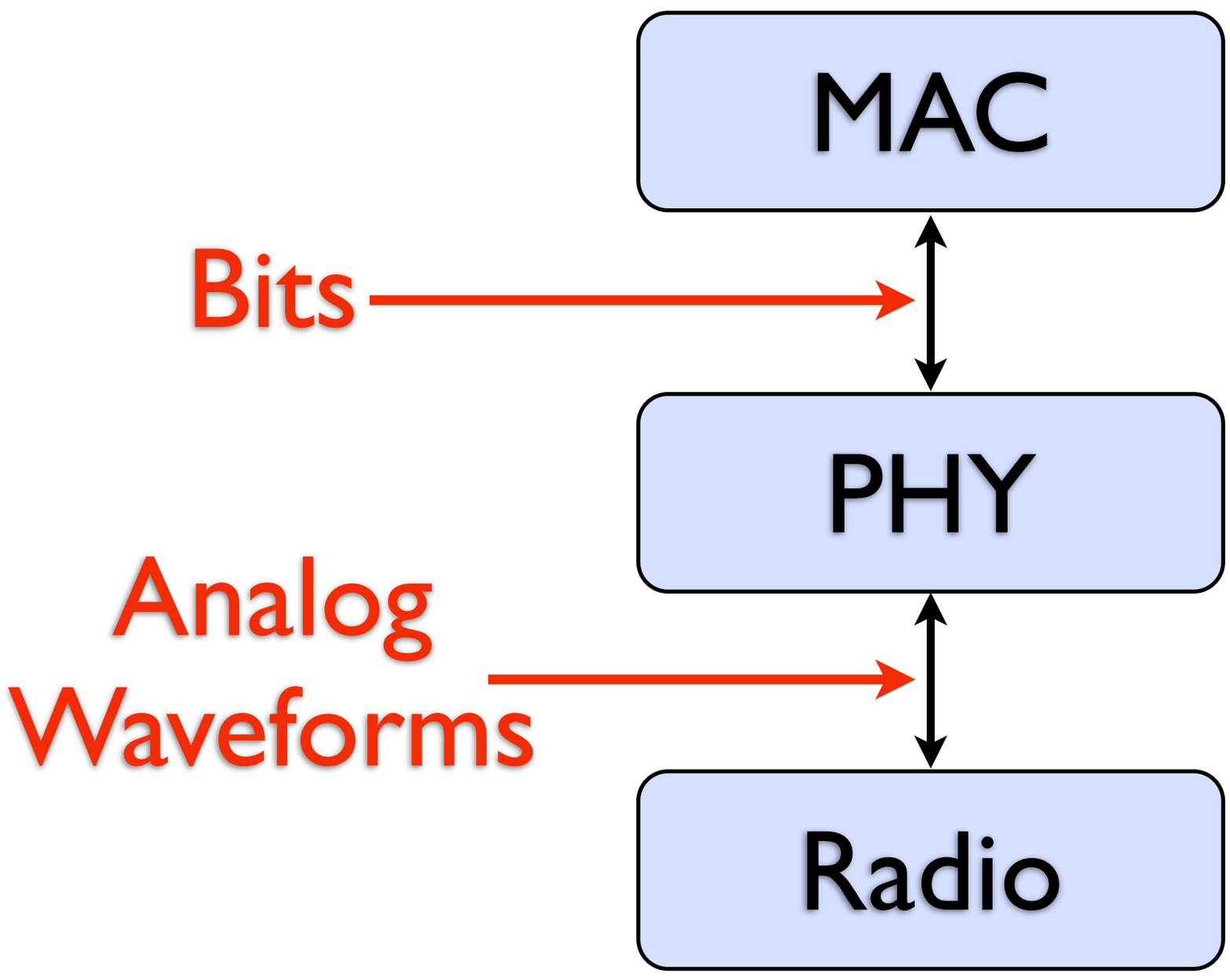
Physical Layer Basics



Physical Layer Basics

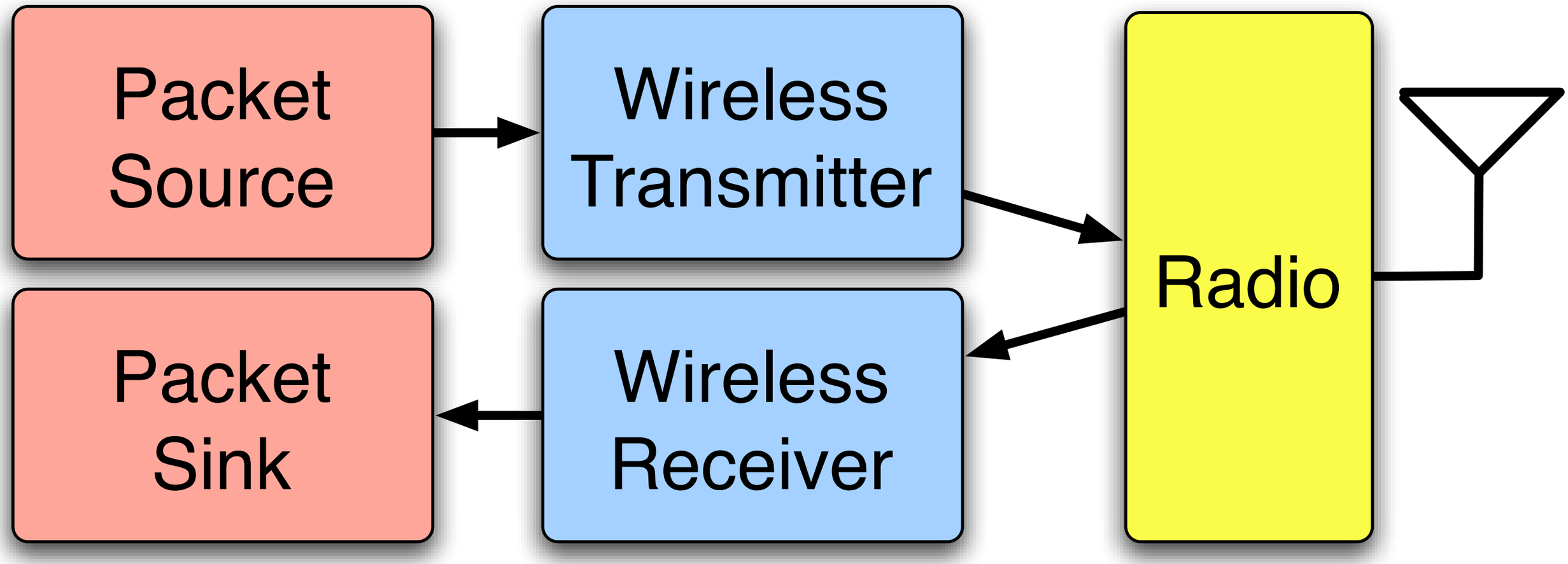


Physical Layer Basics



Physical Layer Basics

Simple Wireless Node



Physical Layer Basics

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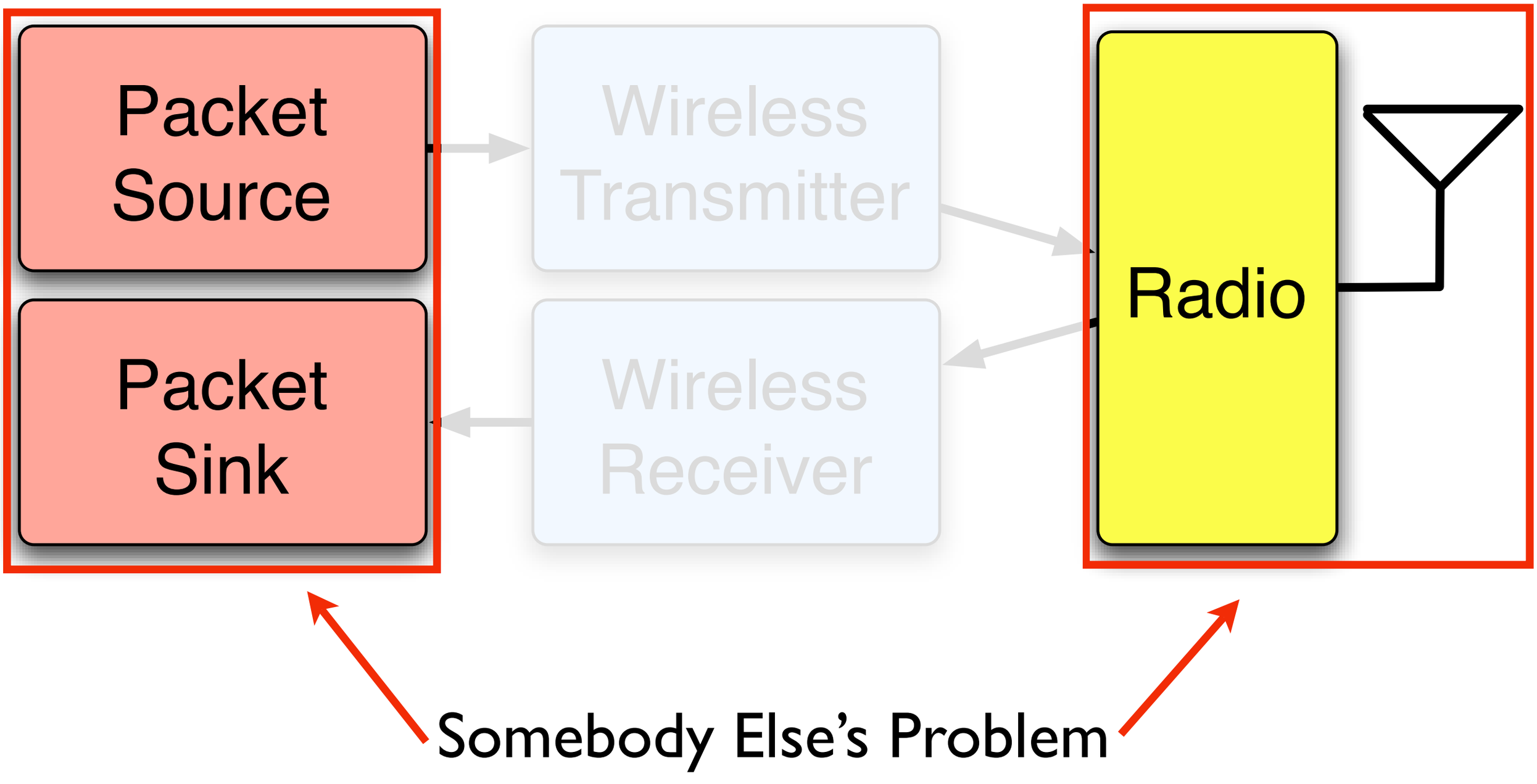

Physical Layer Basics

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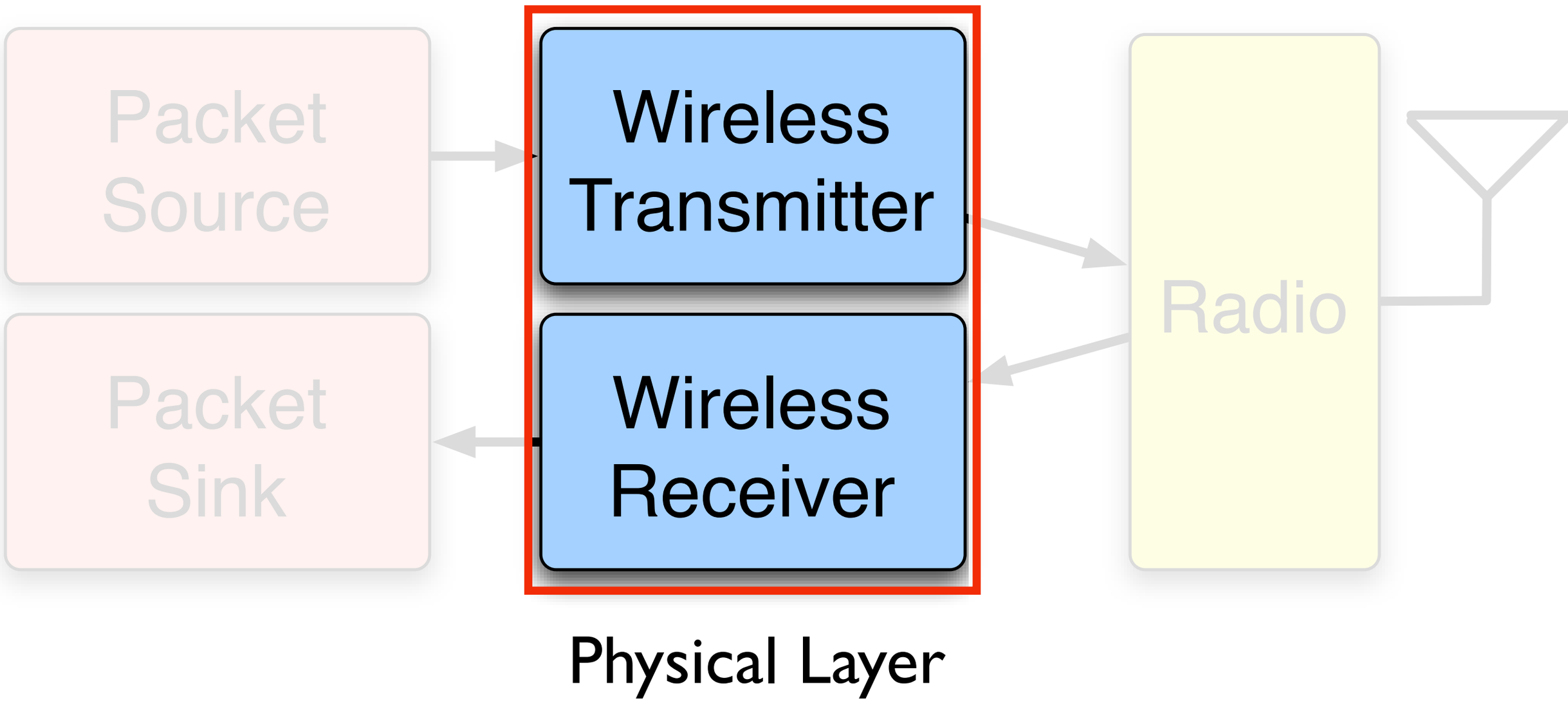

Physical Layer

PHY Design Flows

- WARPLab
  - MATLAB↔WARP Link
    - Very rapid prototyping of PHY algorithms
- Real-time PHY design
  - Low-level FPGA design
  - Putting it all together

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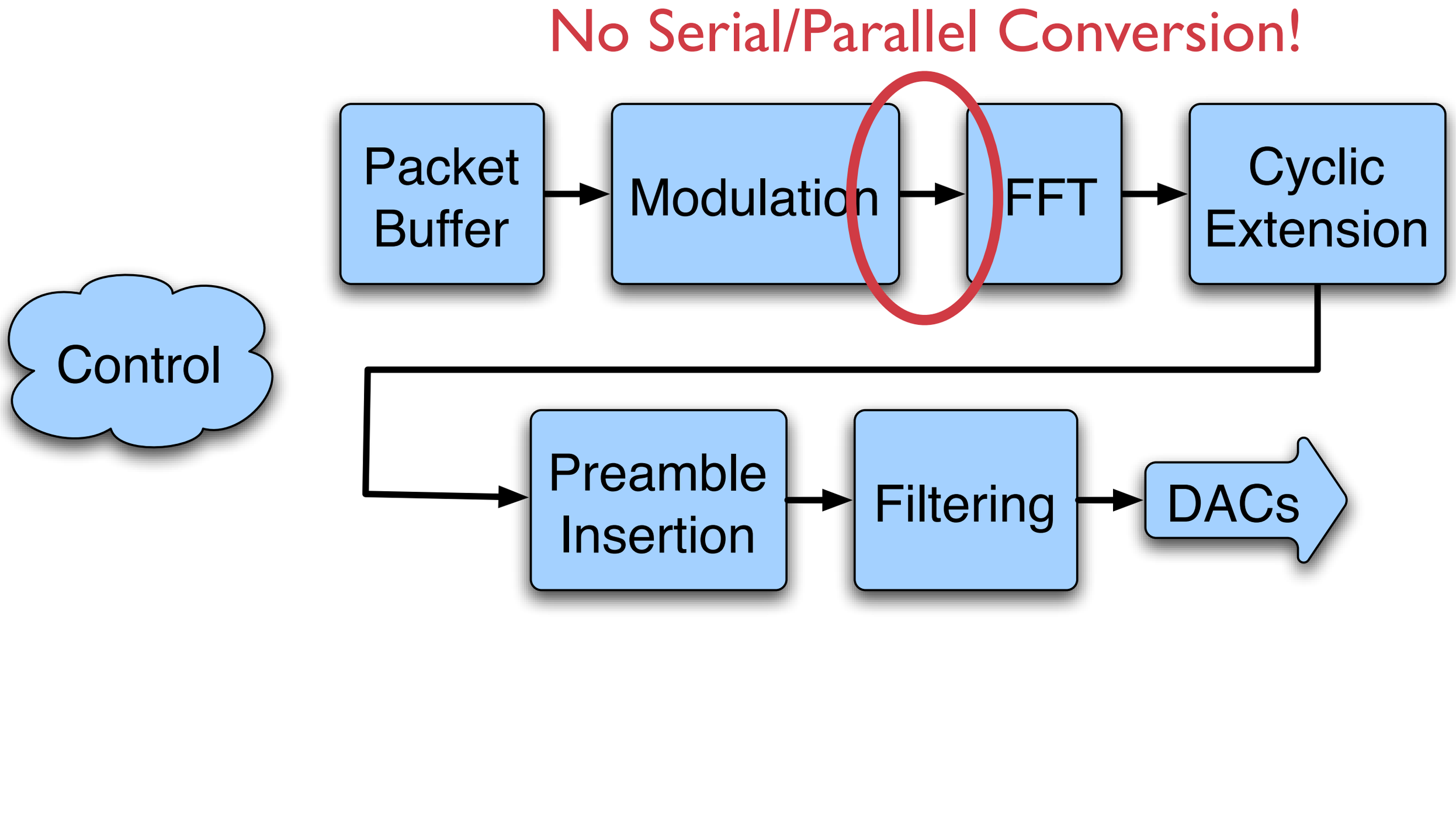
PHY Example: OFDM Tx



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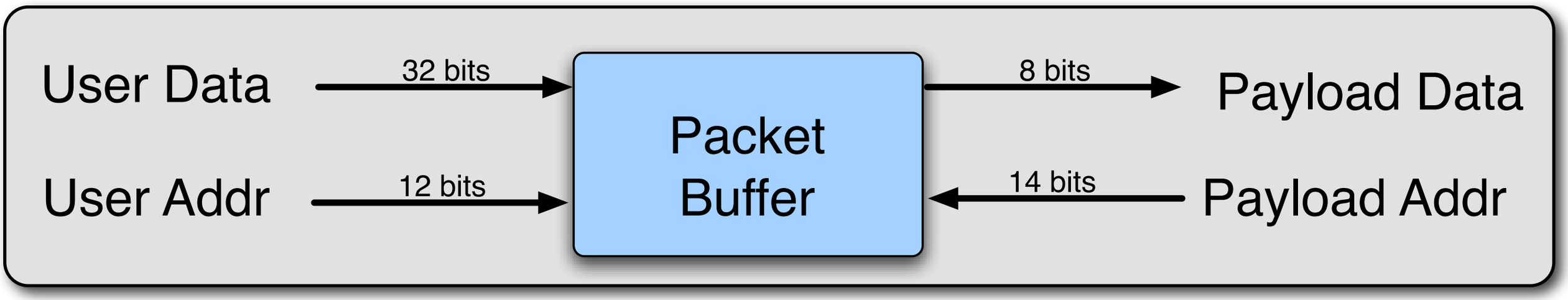
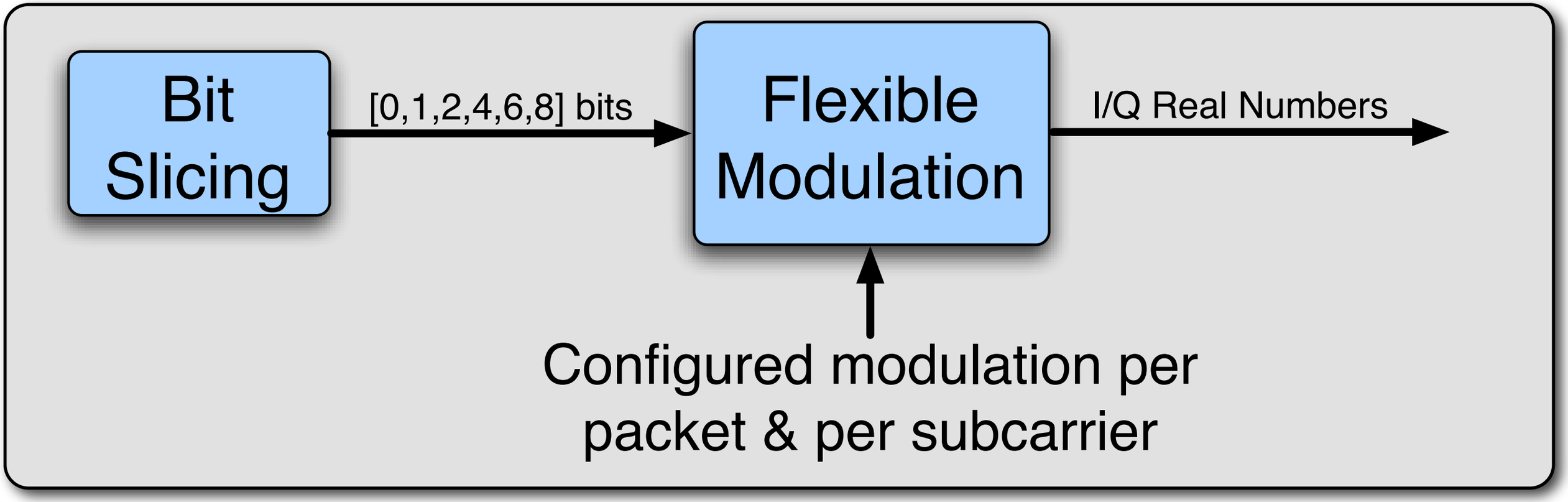
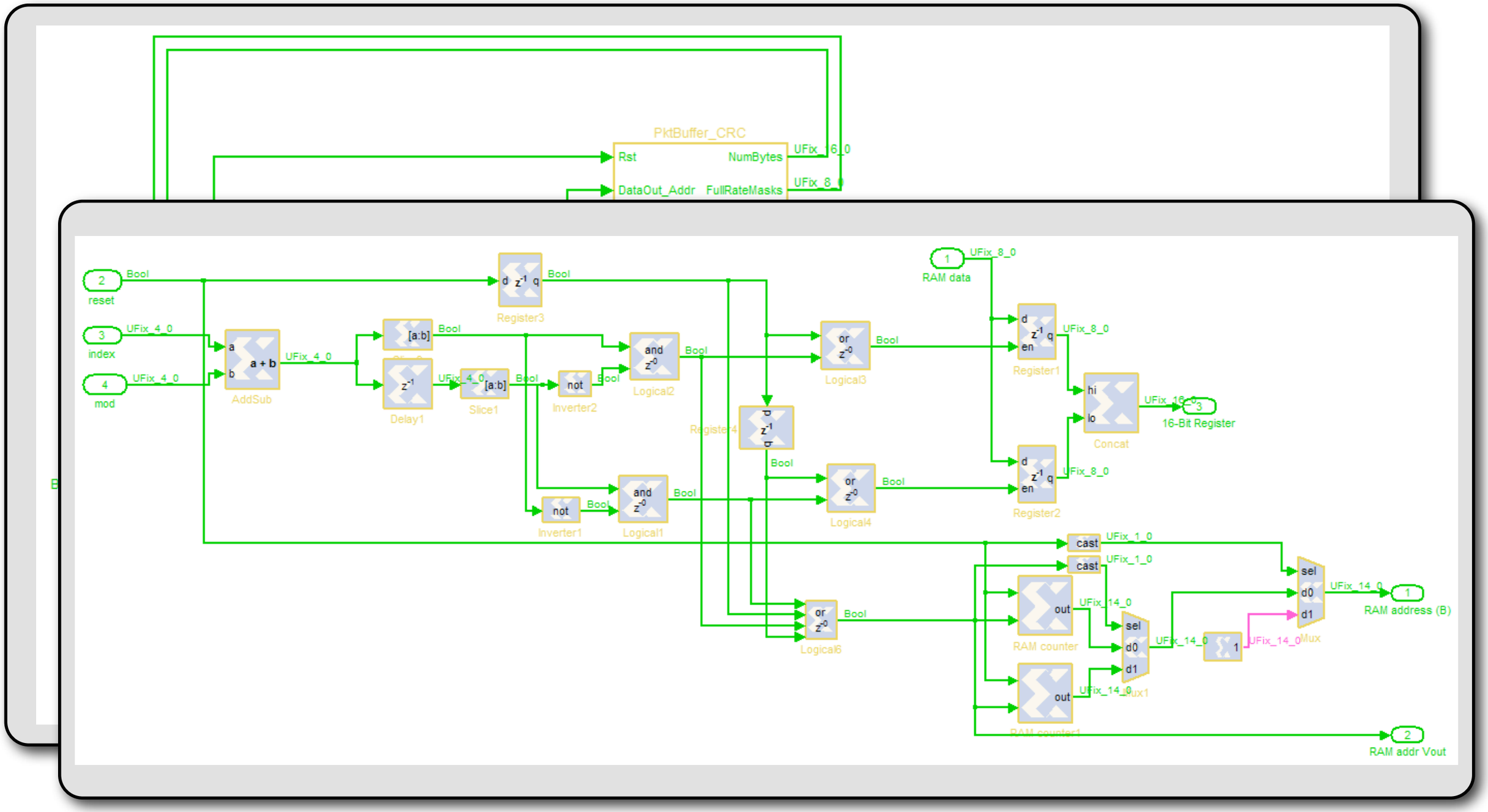


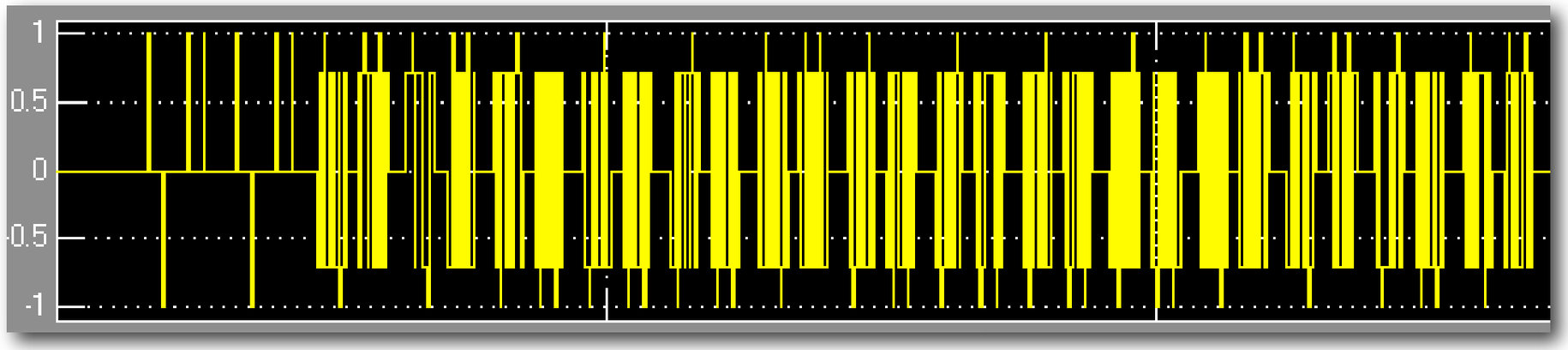


PHY Example: OFDM Tx



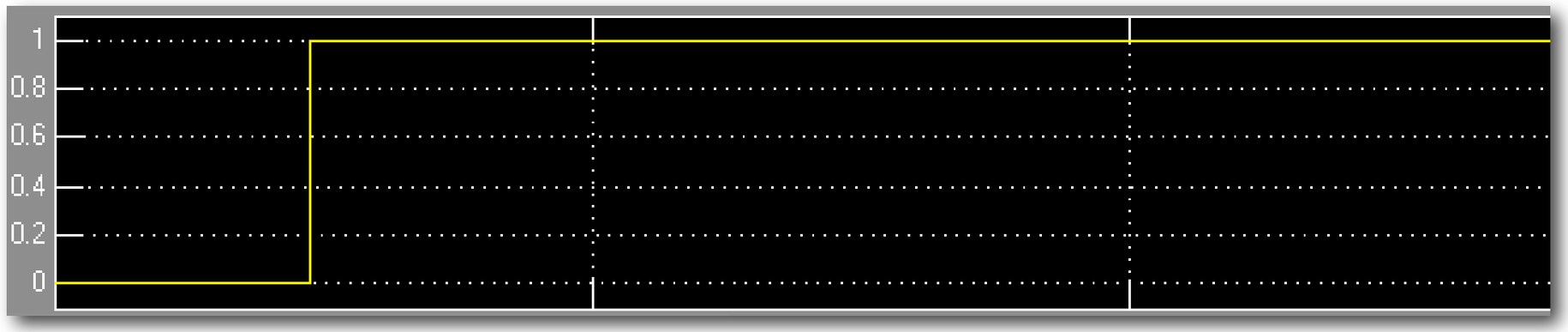
PHY Example: OFDM Tx

Modulator Output

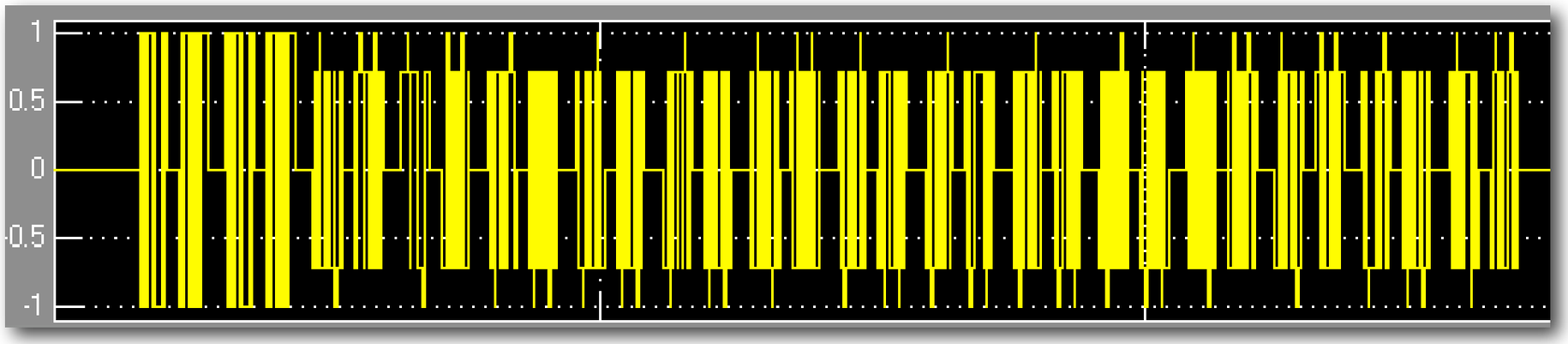


Stored Training Sequence

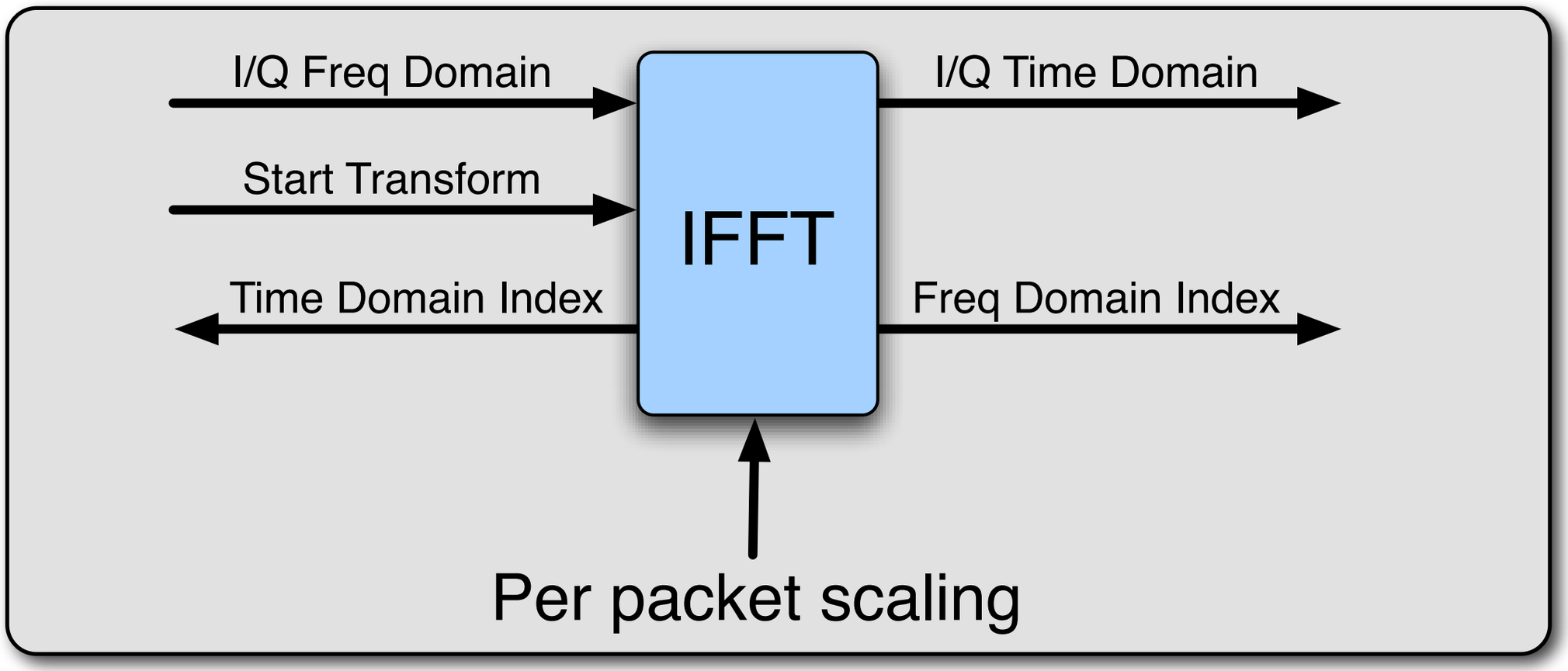
Source Mux Select



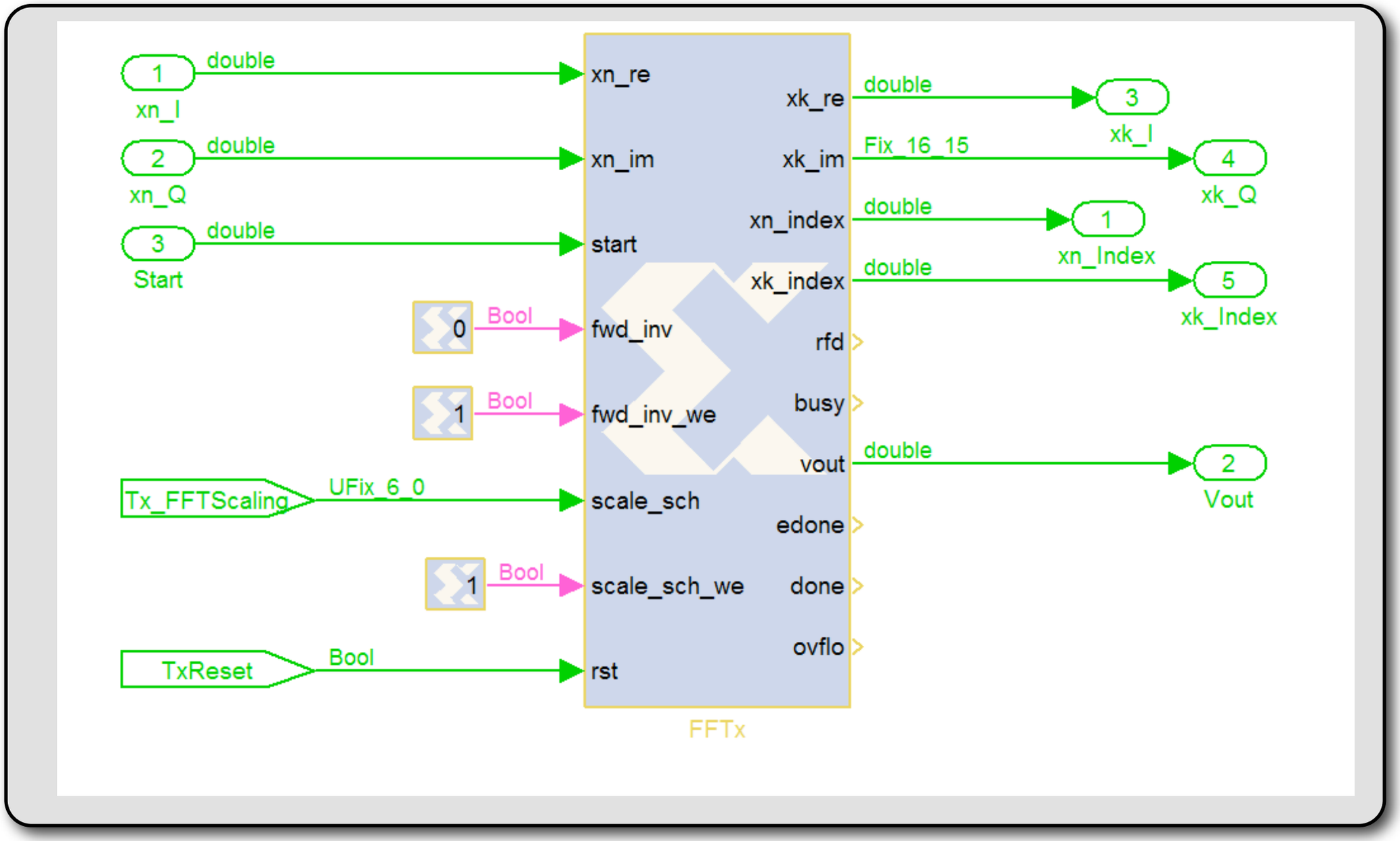
Input IFFT



PHY Example: OFDM Tx



PHY Example: OFDM Tx



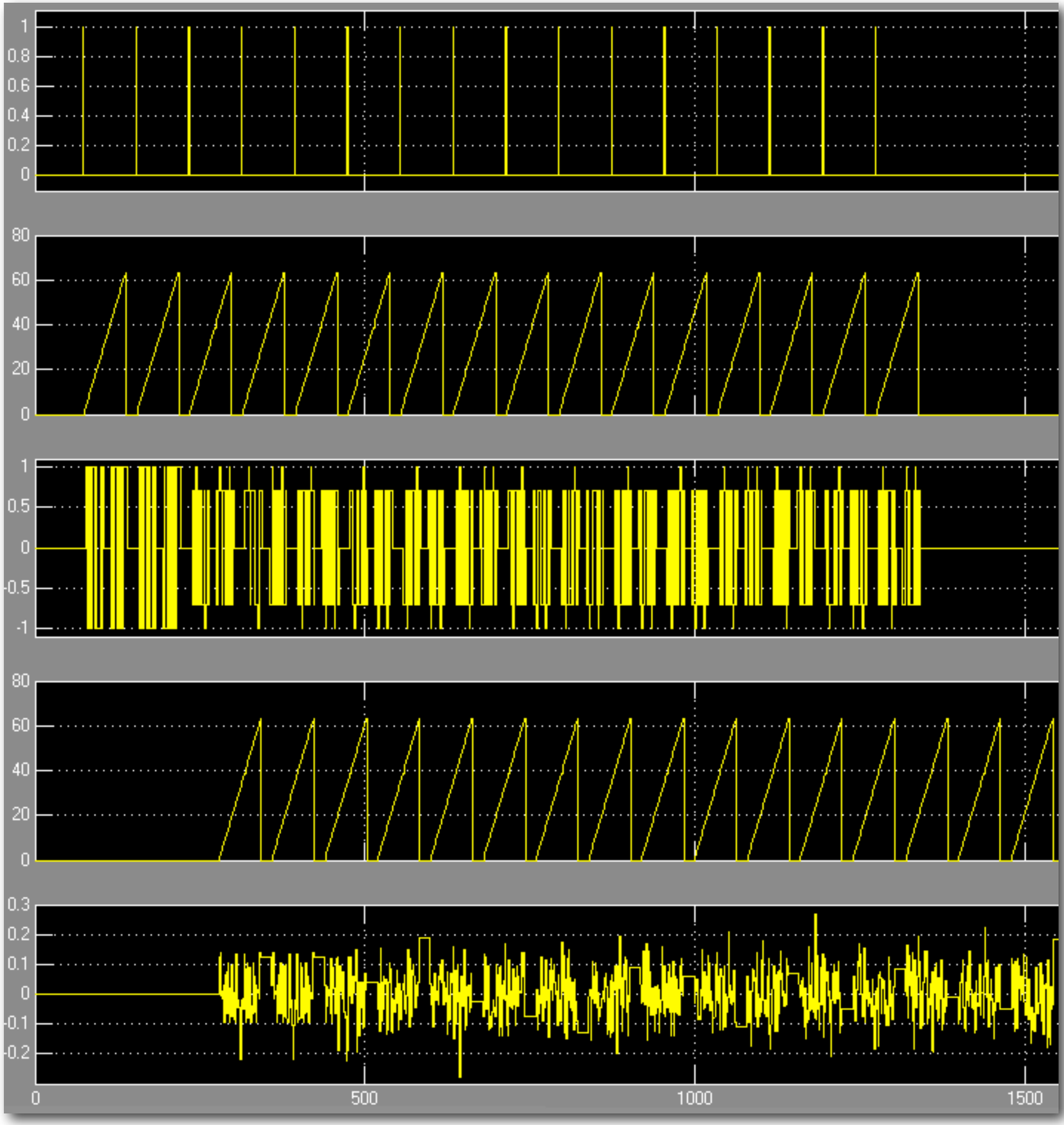
IFFT Start

Input Index

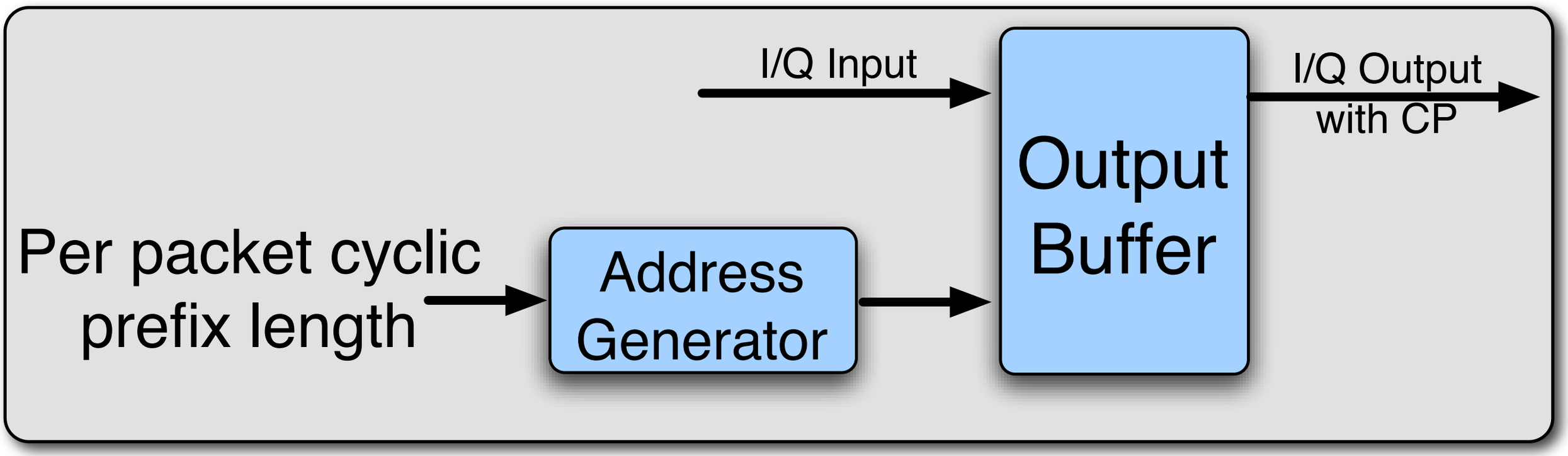
Input Data

Output Index

Output Data



PHY Example: OFDM Tx



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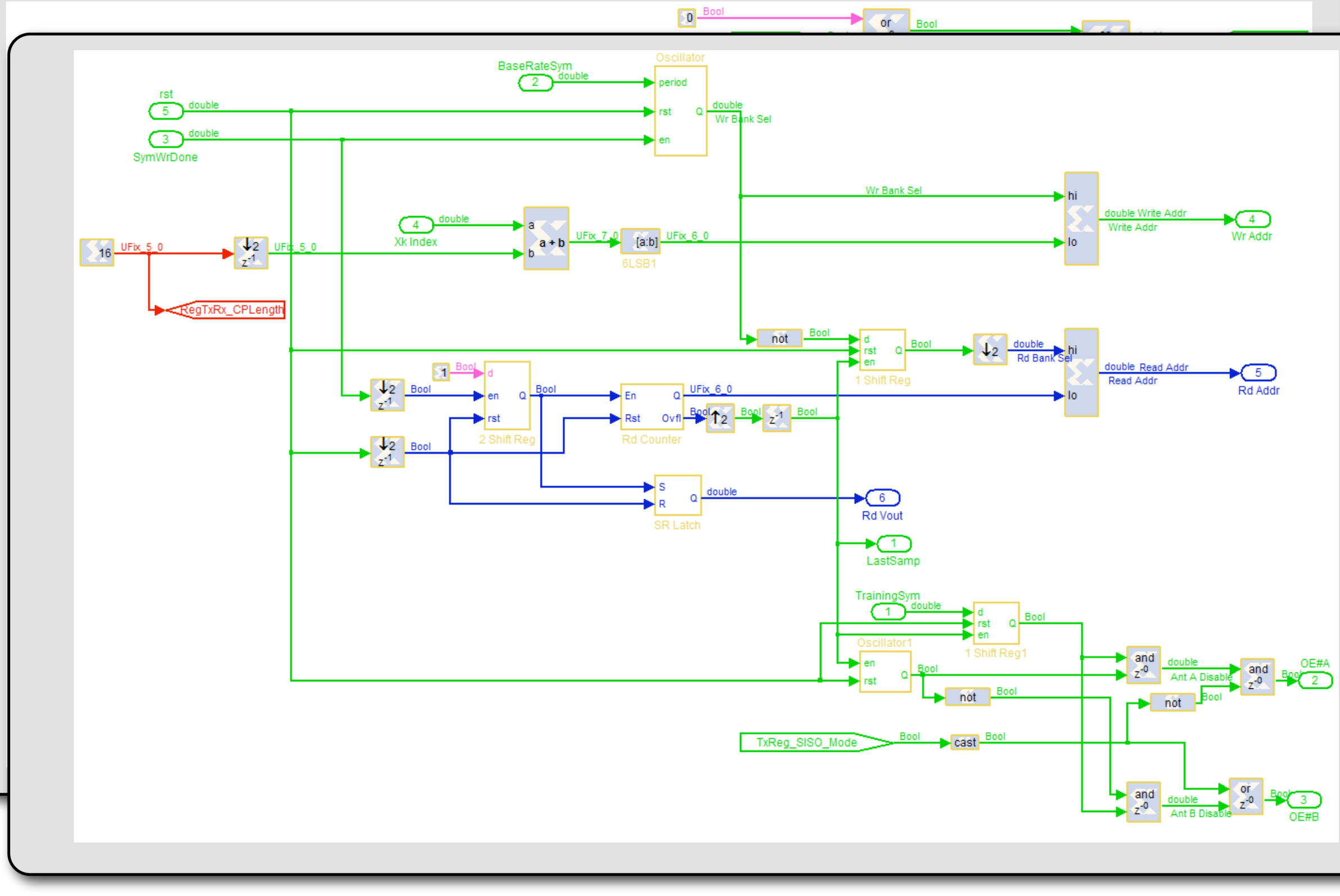
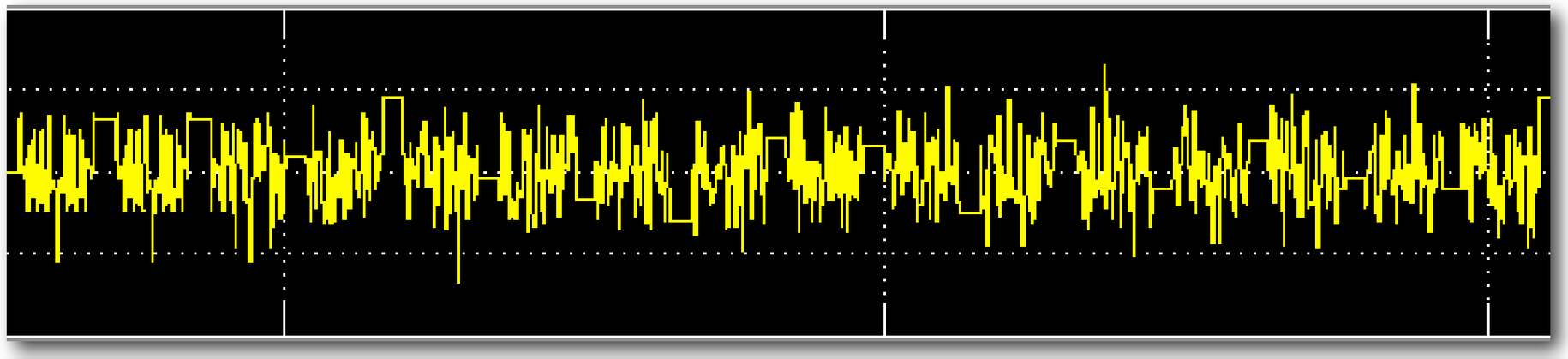
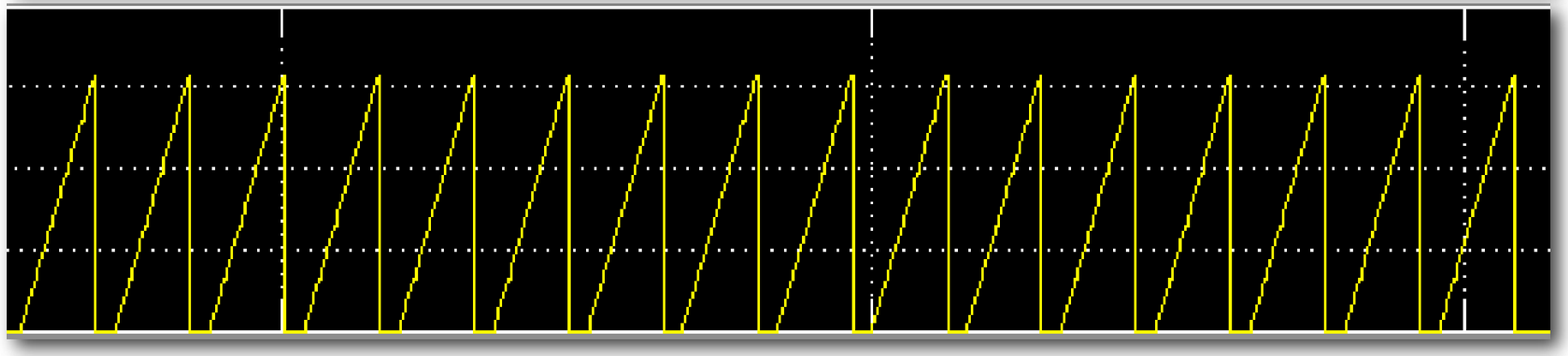


PHY Example: OFDM Tx

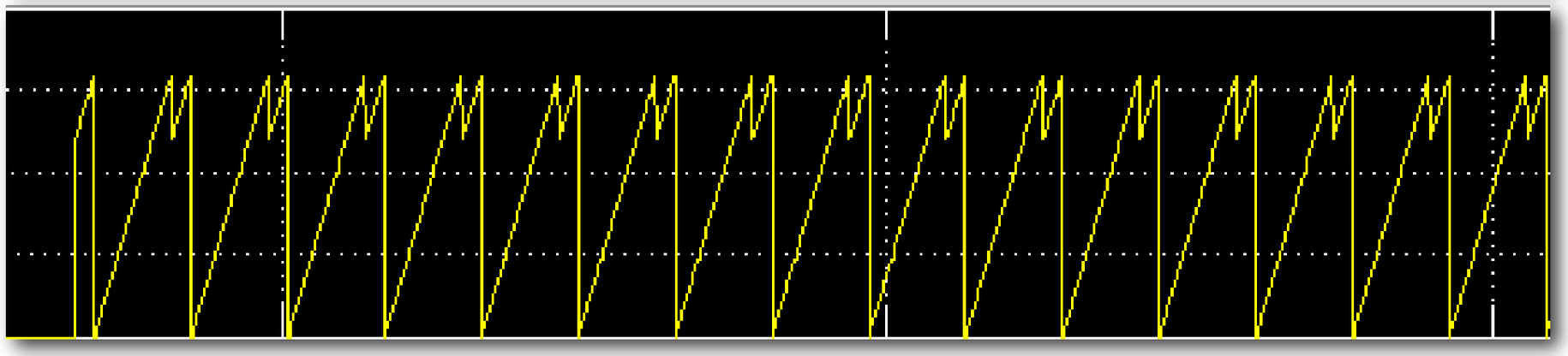
IFFT Output



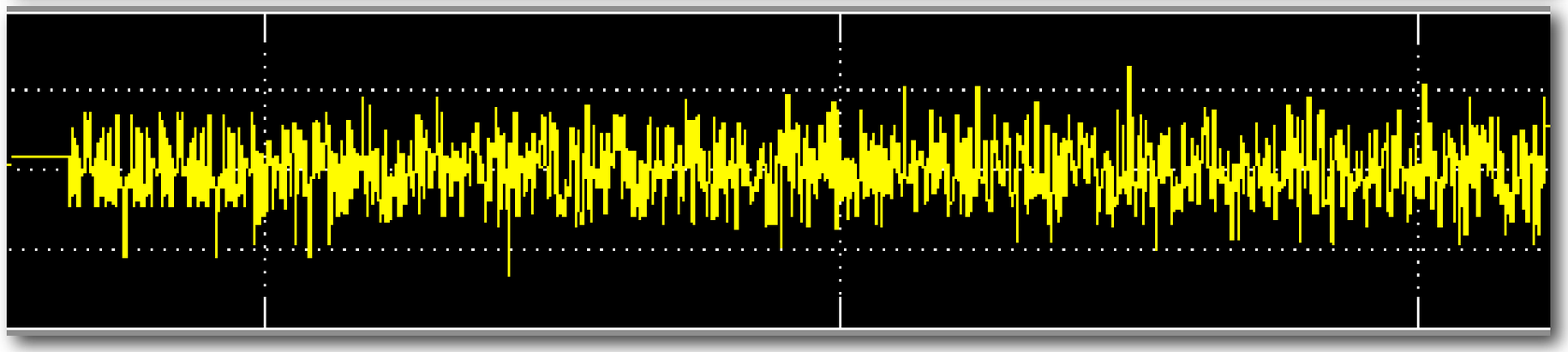
RAM Write Address



RAM Read Address



Cyclically Extended



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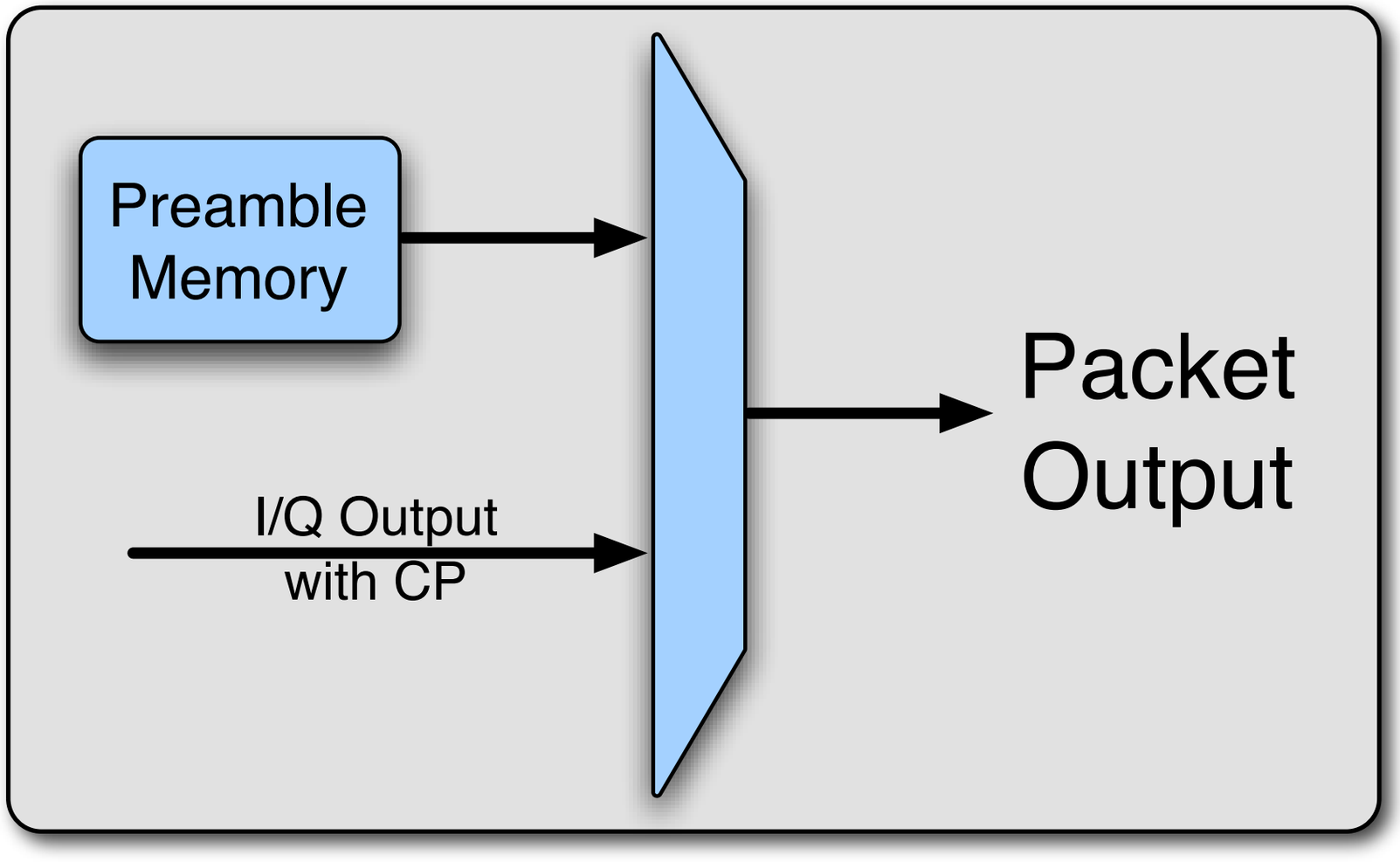
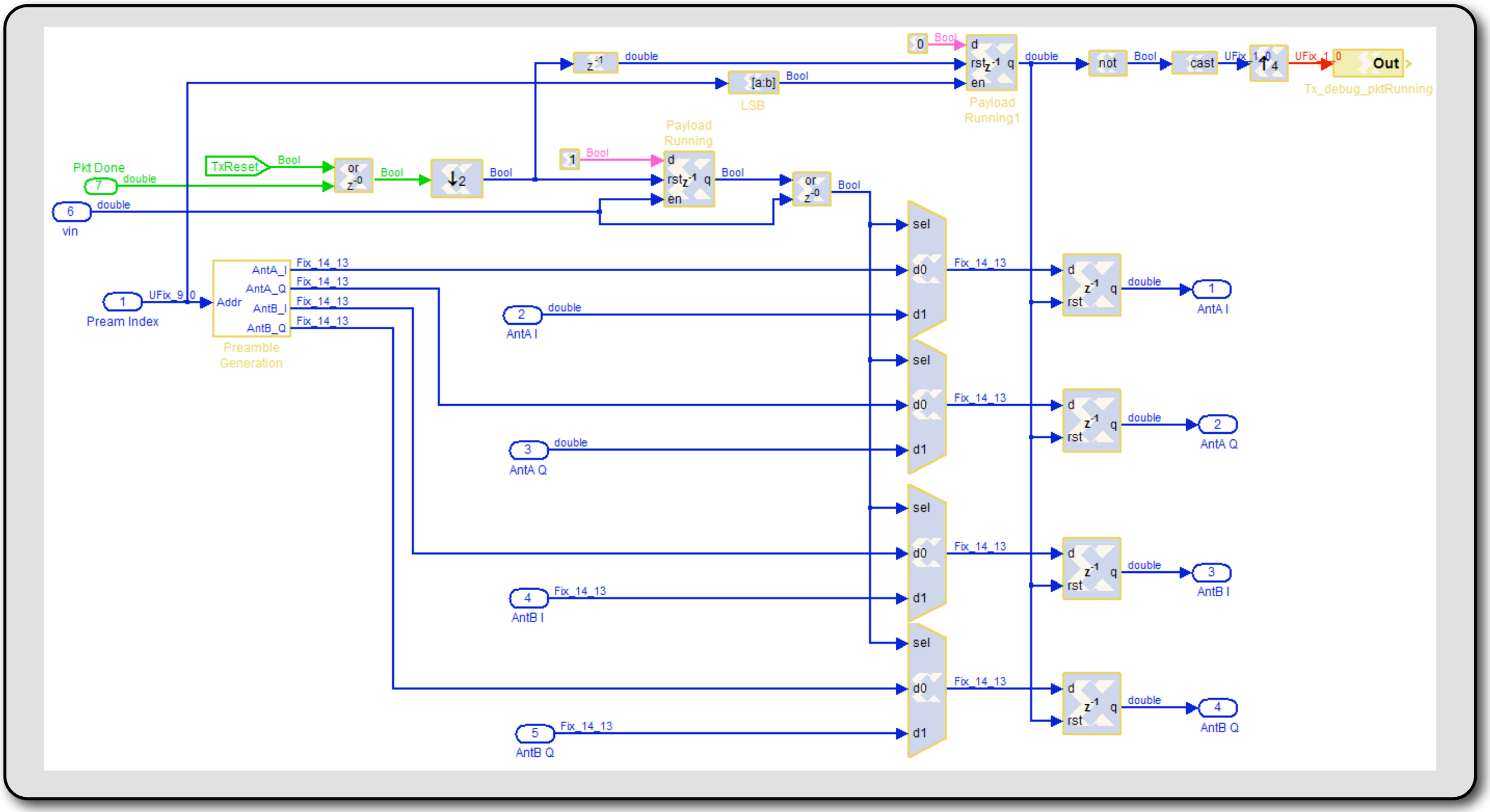
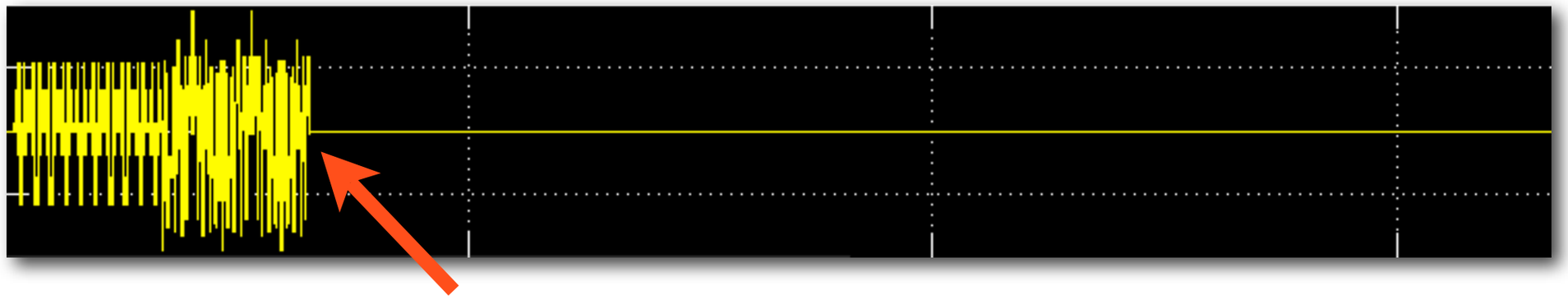


PHY Example: OFDM Tx

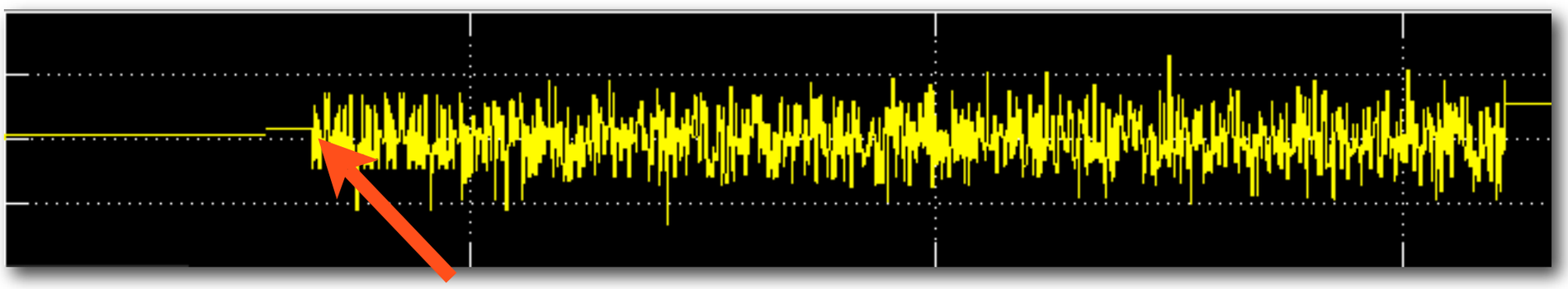


PHY Example: OFDM Tx

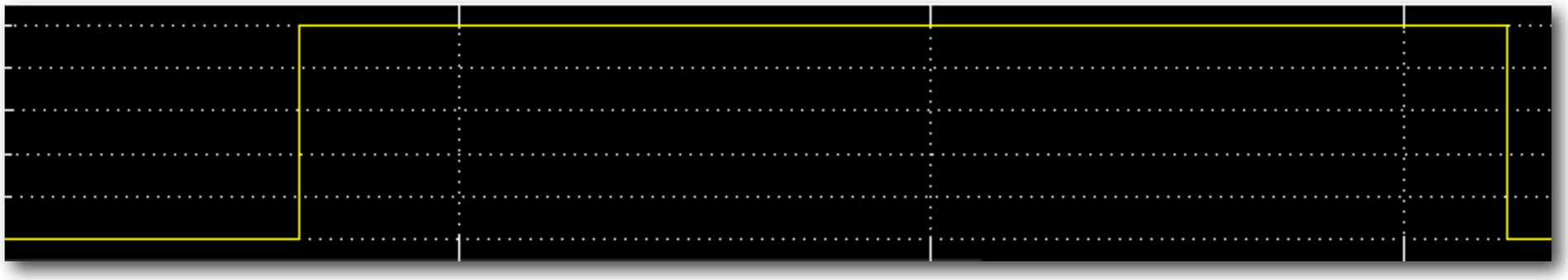
Stored Preamble



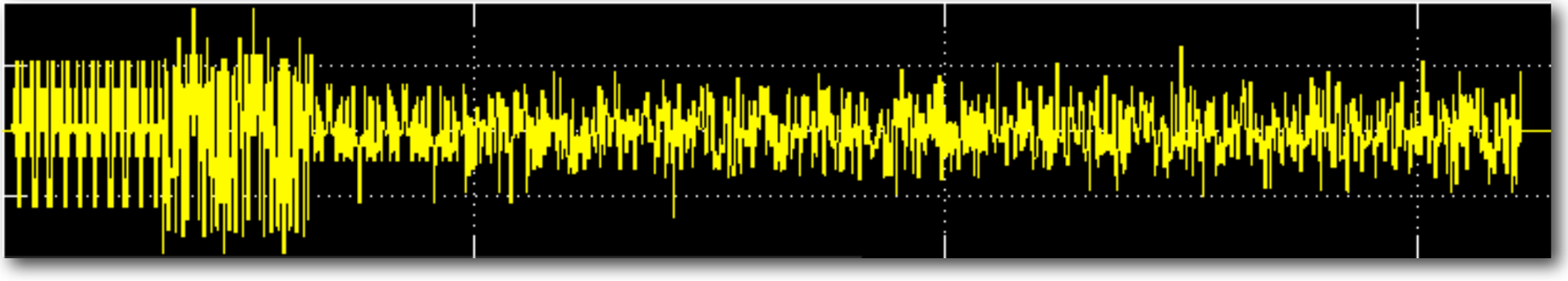
OFDM Output



Output Mux Selection



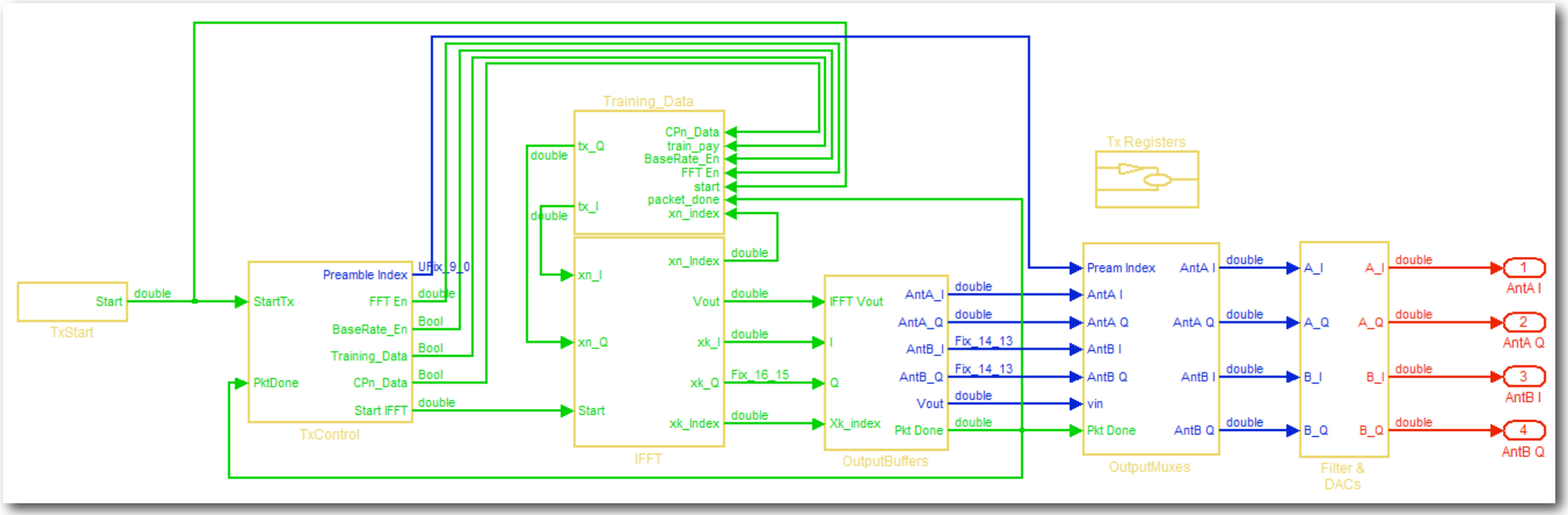
Final Output to DACs



PHY Example: OFDM Tx

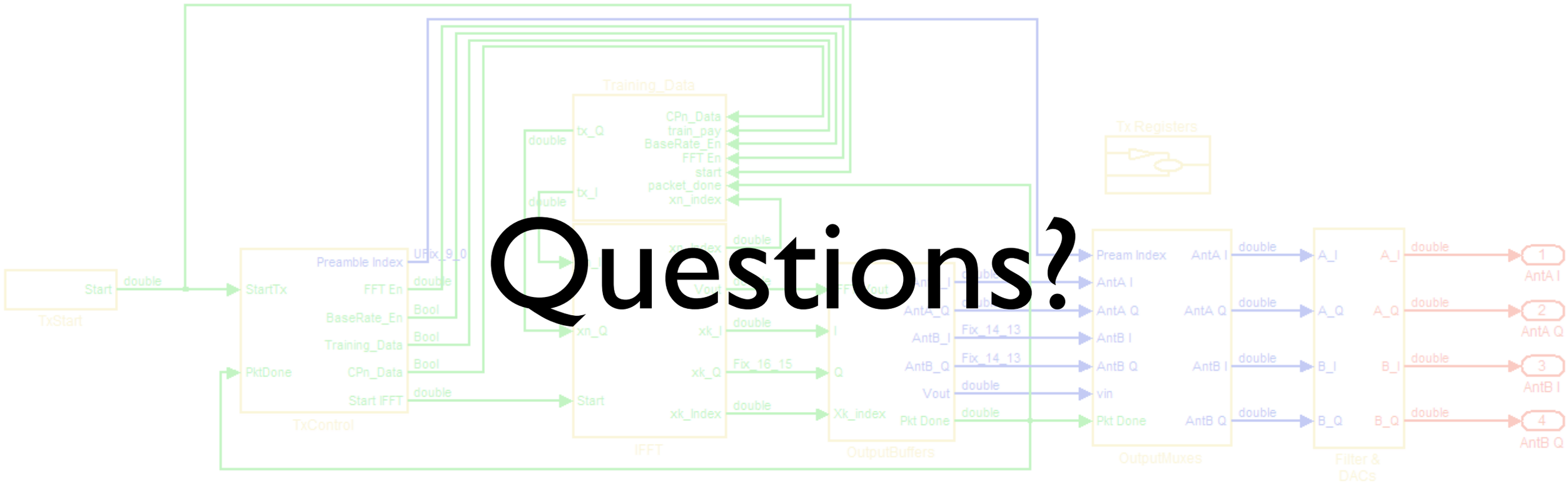
- Per packet configuration drives control system
  - Number of training symbols
  - Number of bytes
  - Modulation choices
- Block specific control blocks
  - IFFT start signal
  - Memory address generation
- Triggers & status between core and PowerPC

PHY Example: OFDM Tx



Complete model is available in the WARP repository

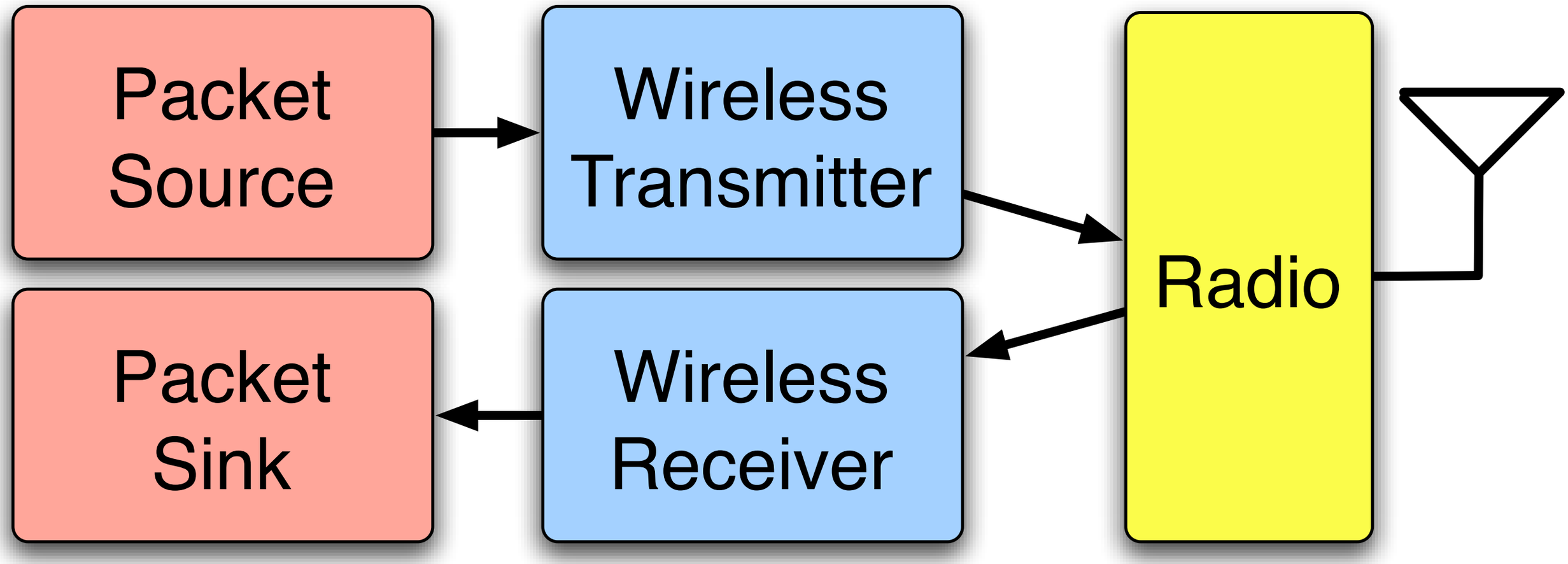
You'll use this model all day tomorrow


Training_Data
CPn_Data
train_pay
BaseRate_En
FFT En
start
packet_done
xn_index
tx_Q
tx_I
double
Tx Registers
Start
TxStart
StartTx
Preamble Index
FFT En
BaseRate_En
Training_Data
CPn_Data
Start IFFT
PktDone
TxControl
Ufix_9_0
Bool
Bool
xn_Q
xn_I
Start
IFFT
xk_Q
xk_I
xk_Index
Fix_16_15
Q
I
Xk_index
OutputBuffers
AntB_I
AntB_Q
Vout
Pkt Done
Fix_14_13
Pream Index
AntA I
AntA Q
AntB I
AntB Q
vin
Pkt Done
OutputMuxes
A_I
A_Q
B_I
B_Q
Filter &
DACs
1
AntA I
2
AntA Q
3
AntB I
4
AntB Q

Questions?

Physical Layer Basics

Simple Wireless Node



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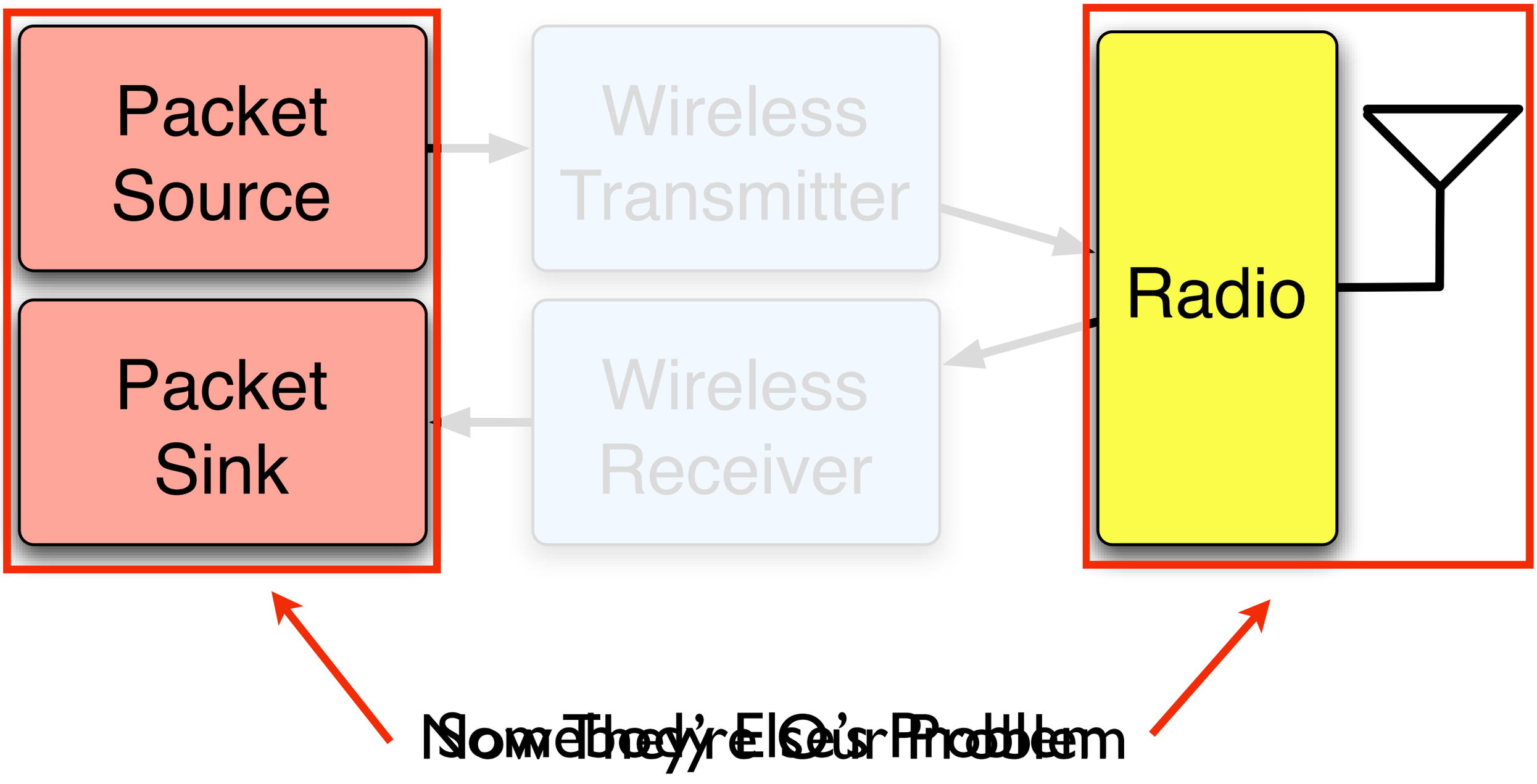
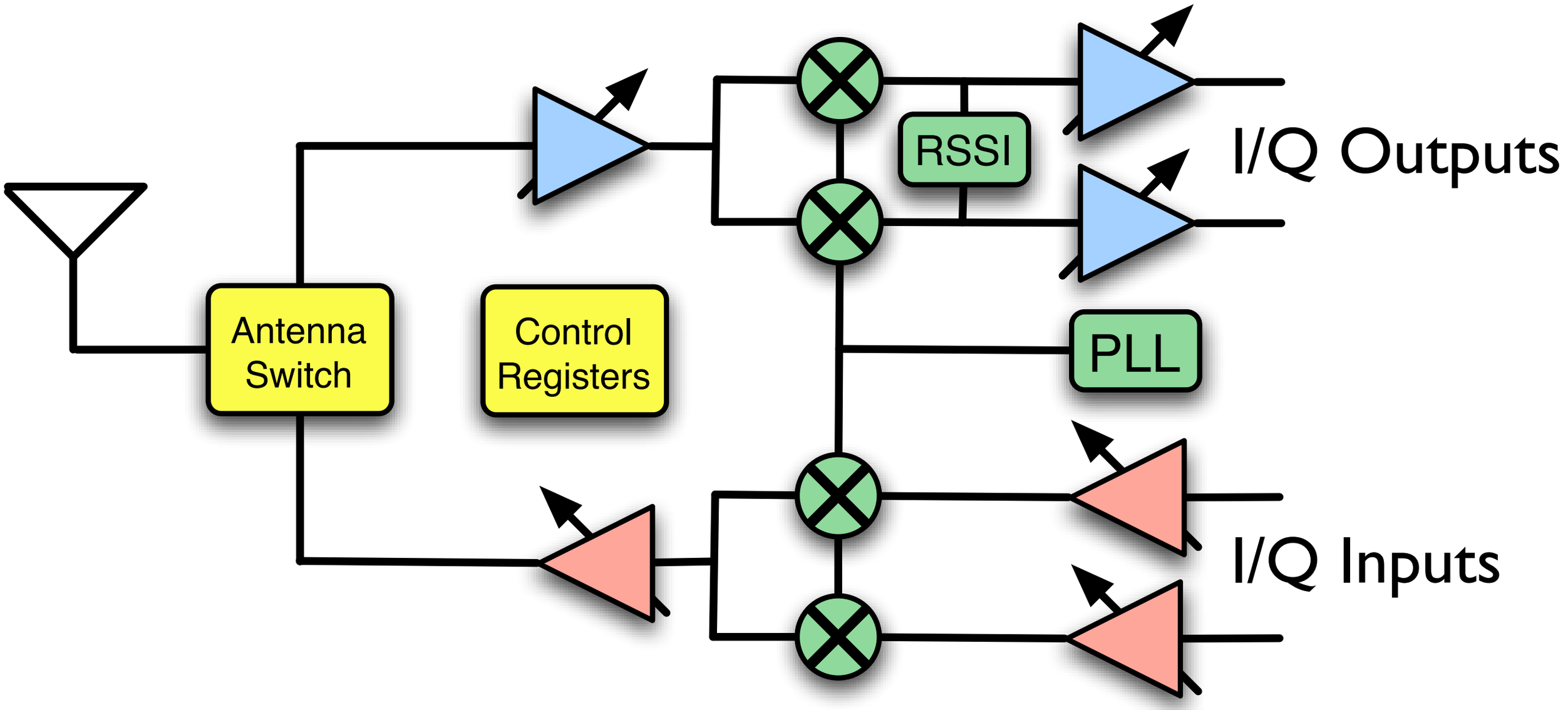


Radio Transceiver



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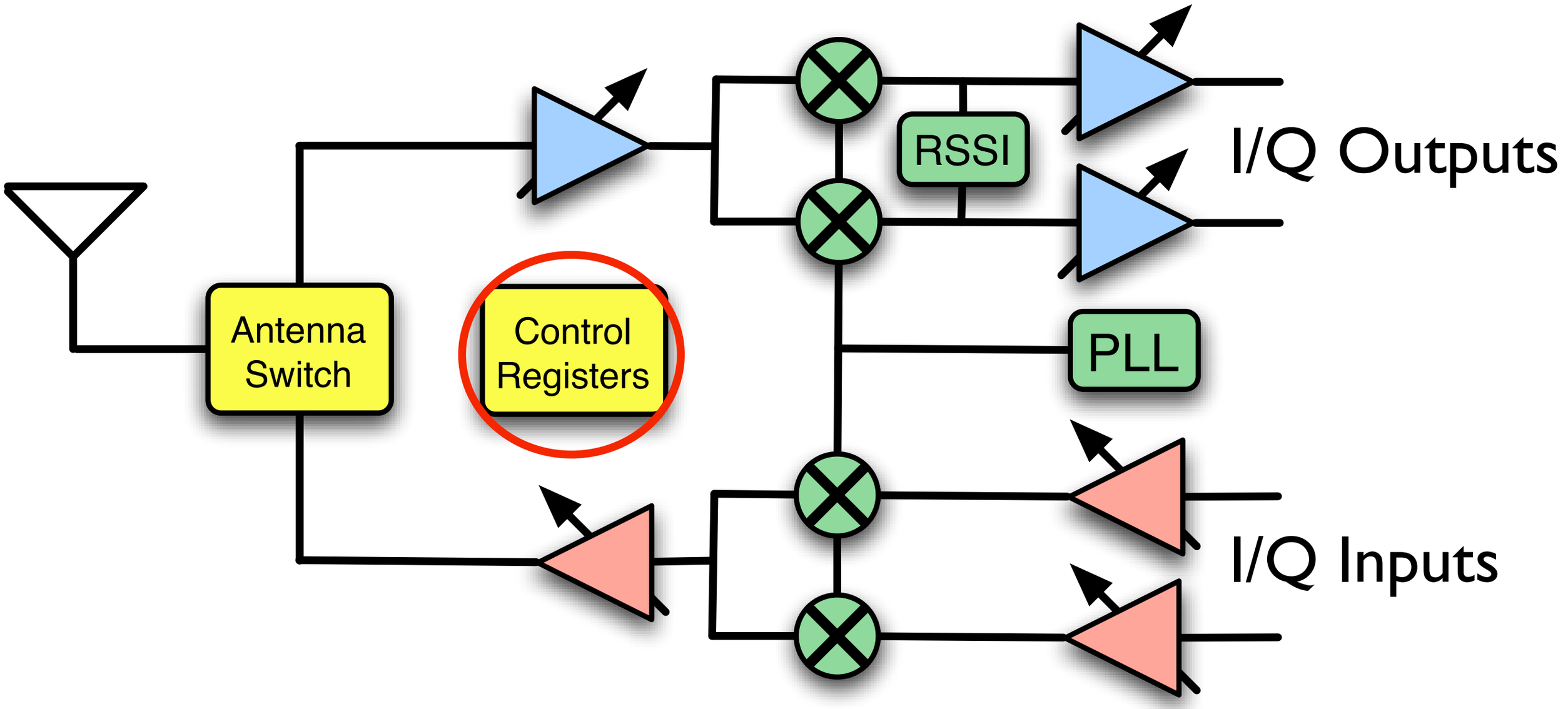
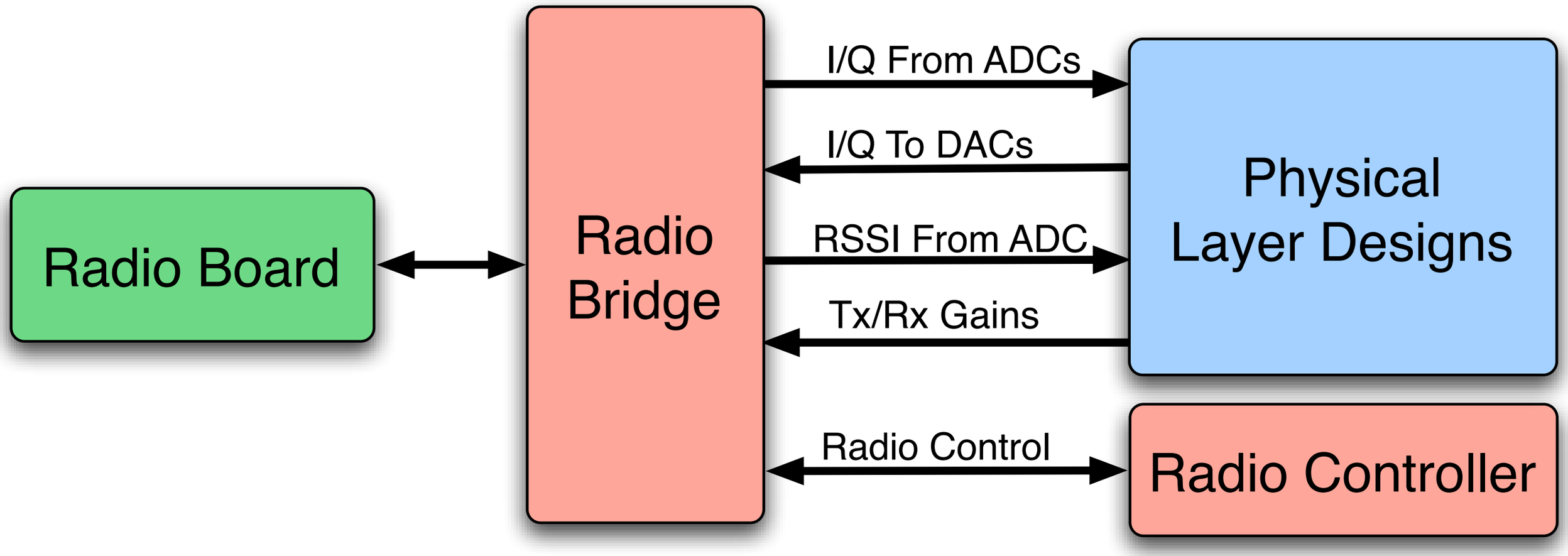
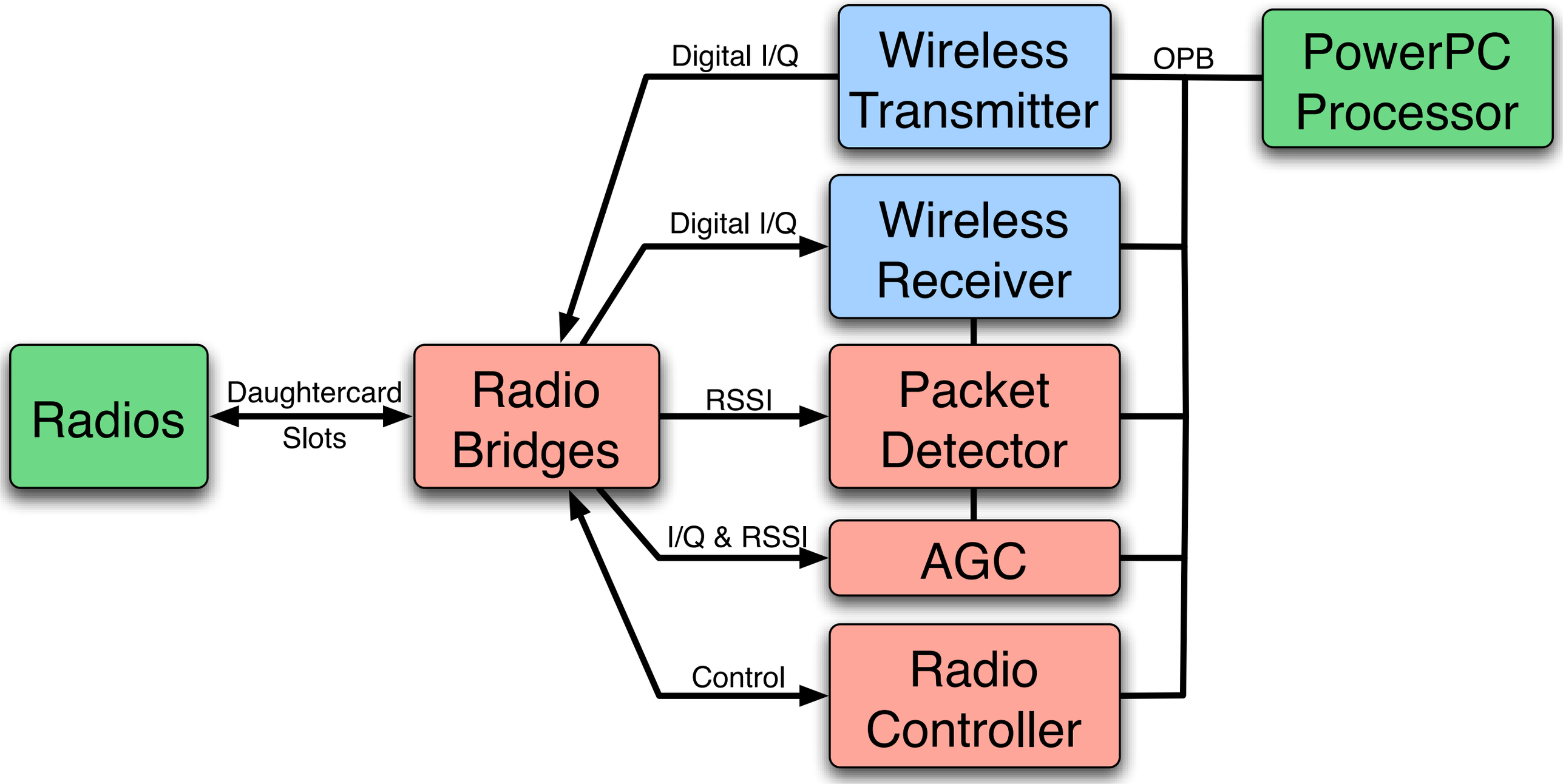


Register Bank
(controlled by SPI interface)

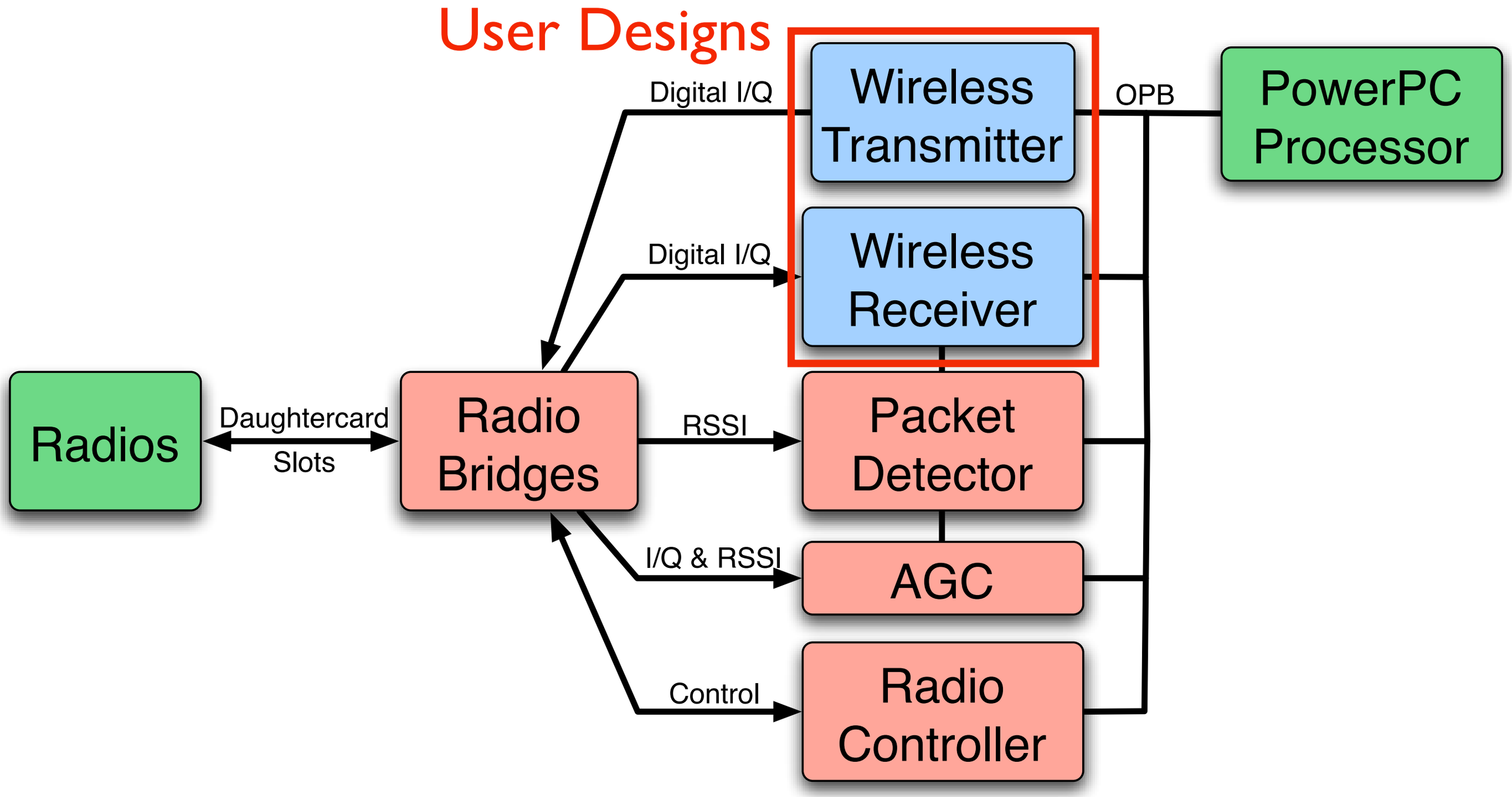
Physical Layer in Hardware



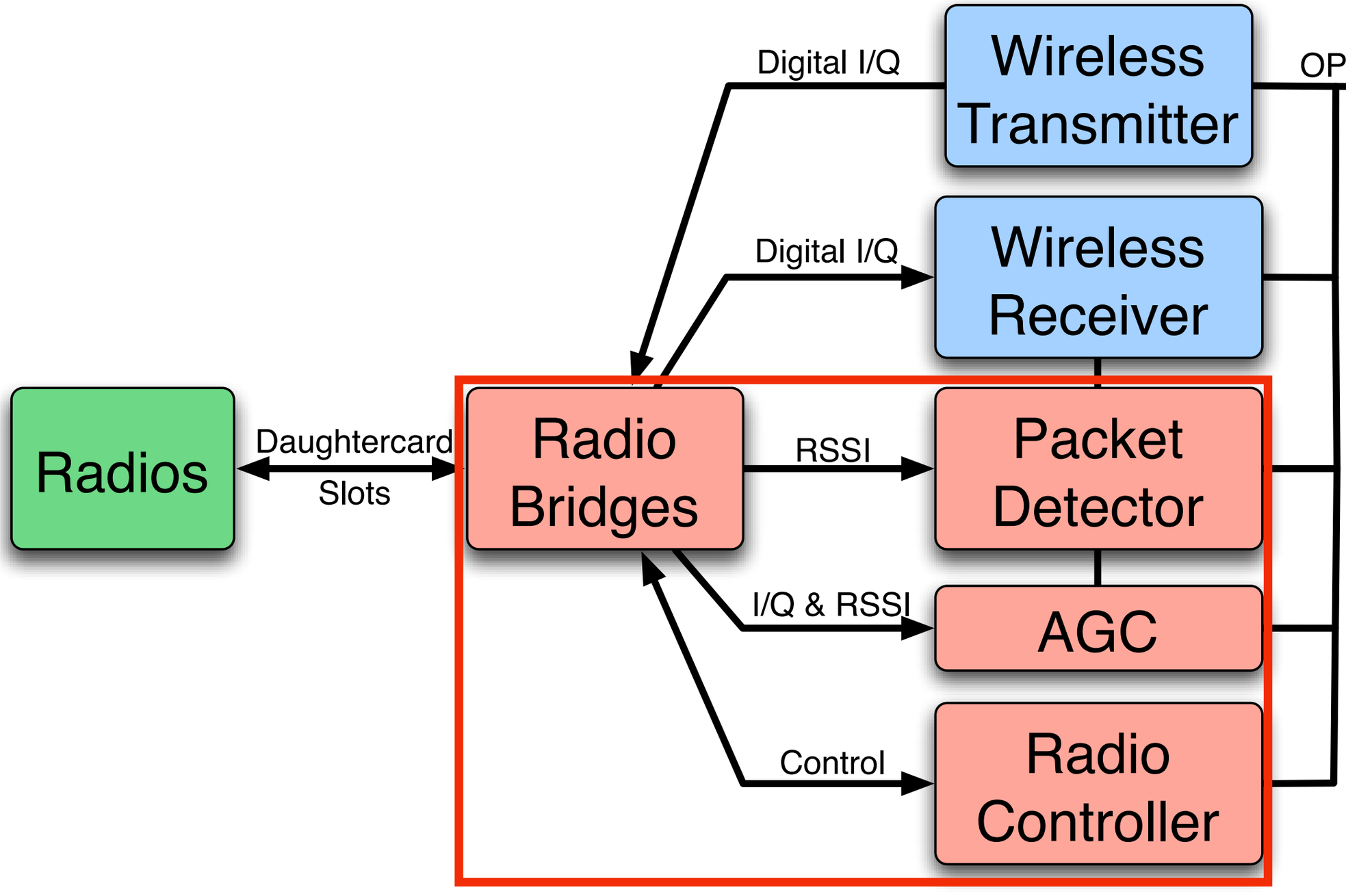
Physical Layer in Hardware



Physical Layer in Hardware

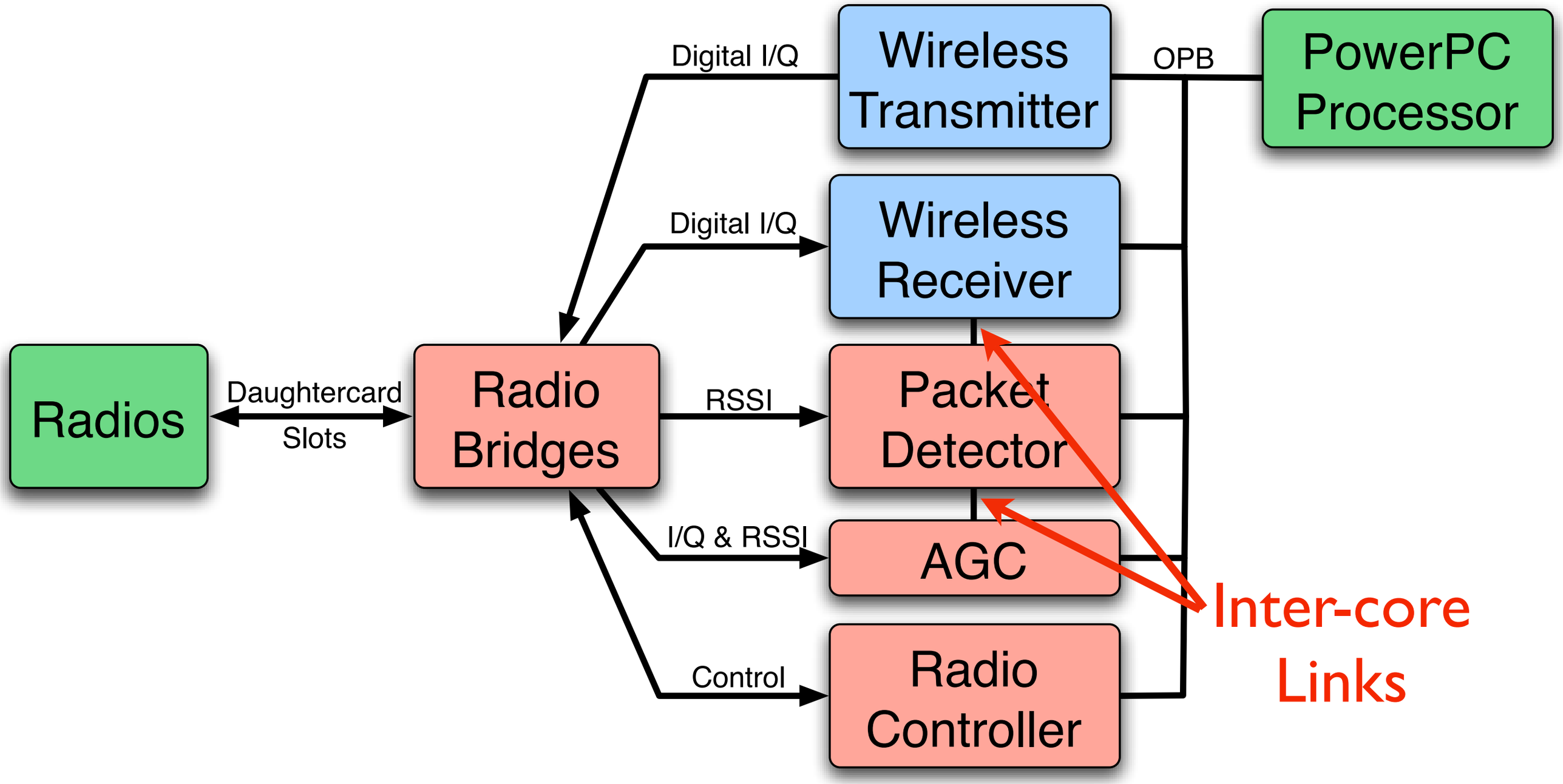


Physical Layer in Hardware



Platform Support Packages

Physical Layer in Hardware



Packet Detection

- Triggers AGC & receiver models
- Detection based only on received energy
  - I/Q saturated and too corrupted
  - Gain adjusted *after* detection
- Detection confirmed/rejected by Rx PHY
  - Requires some data-aided detection
  - Correlates against every packet's preamble

RSSI

Incoming Packet

700
600
500
400
300
200
100
0

0
500
1000
1500
2000
2500
3000
3500

Radio Controller

- Controller hardware
  - I/O registers & SPI controller
  - One core controls all 4 radios & DACs
- Controller software
  - Full C API for radio board control
  - All radio features controlled by C functions
  - Simple functions required
  - Advanced functions optional

Radio Controller API

```
WarpRadio_v1_Reset()

WarpRadio_v1_TxEnable()
WarpRadio_v1_SetCenterFreq2GHz()
WarpRadio_v1_BaseBandTxGain()
WarpRadio_v1_TxVGAGainControl()
WarpRadio_v1_24AmpEnable()

WarpRadio_RxEnable()
WarpRadio_RxLNAGainControl()
WarpRadio_RxVGAGainControl()
WarpRadio_RxLpfCornFreqCoarseAdj()
```

Radio Controller API

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WarpRadio_RxVGAGainControl()
WarpRadio_RxLpfCornFreqCoarseAdj()

Full API online:

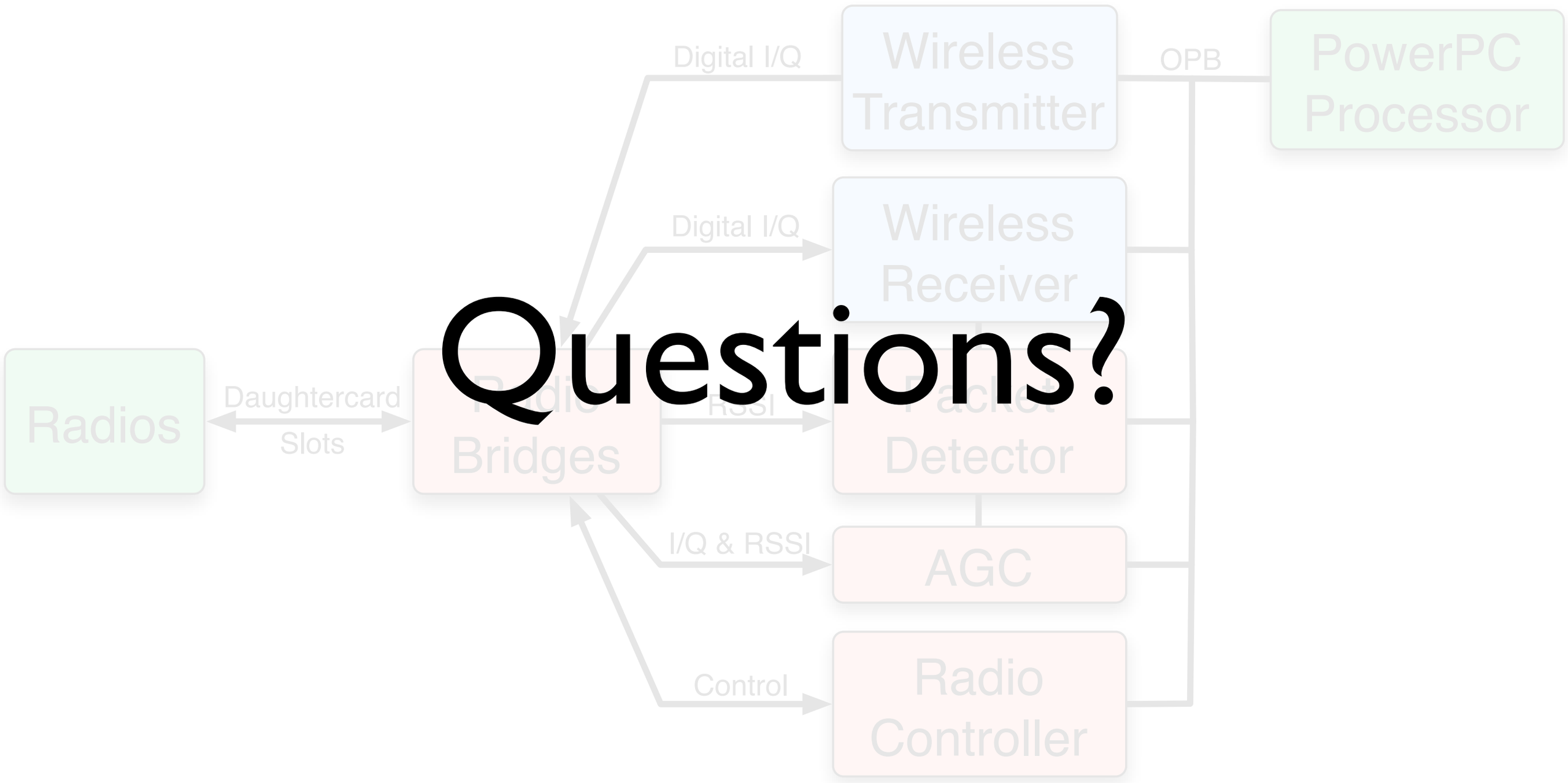
http://warp.rice.edu/WARP_API

Radio Bridge

- Ties user designs to radio hardware
  - Ports for user signals (ADC, DAC, gains)
  - Ports for radio controller I/O
- Users instantiate one bridge per radio board
- All constraints & most links are automatic
- Custom Verilog peripheral

PHY Design Review

- Build & verify PHY in FPGA design tool
  - System Generator is a good choice
  - Make sure everything works in simulation
- Generate simple Tx/Rx peripherals
  - “Cheating” is good at first
- Hook up your core in the EDK
  - Use the radio bridges & controller
- Generate the platform & test it in hardware


Digital I/Q
Wireless Transmitter
OPB
PowerPC Processor
Digital I/Q
Wireless Receiver
Radios
Daughtercard Slots
Radio Bridges
RSSI
Packet Detector
I/Q & RSSI
AGC
Control
Radio Controller

Questions?

Lab 3: Simple Transmitter

- Build a sinusoid generator in Sysgen
- Convert the model to a PLB peripheral
- Connect the Tx core to the radio bridge
- Test the model at RF