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Date: January 25, 2013

M.Sc. Thesis report within Electronics Design
30hp

Power Control Mechanisms on WARP boards

EL007A

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ABSTRACT

In recent years, a number of power control concepts have been studied and implemented either in simulation or in practice for different communication systems. It is still the case that a great deal of research is being conducted within the area of energy efficient power control mechanisms for future wireless communication network systems. However, only a limited amount of practical work has been implemented on real test beds environment. The main goal of this thesis is to propose and develop new prototype Transmit Power Control Mechanisms (TPCM) on WARP (Wireless Open-Access Research Platform) boards for point-to-point communications, which are to be developed and tested in an indoor environment. This work mainly focuses on the automatic power control nodes, transmission and reception over-the-air. In this thesis, we have designed and developed TPCM to adjust the power levels on a transmitter node by following the feedback (ACK) approach. In this case, the destination (receiver) node always sends the feedback (ACK) to transmitter node during every successful transmission of message signal and the main focus is on a reduction in the packet loss rate (PLR), an increase in the packet reception rate (PRR) and the capacity of the nodes. In this real work, we have developed and measured the results based on two functions namely, with and without packet window function power control mechanisms.

According to the measurements section, both with and without function power control mechanisms proved to have better performances for different tunable parameters. If both functions are compared, then the with window function power control mechanism was shown to produce better performances than the without window power control mechanism and it also converged faster than the without window function. If consideration was given to controlling a reduction in packet loss rate, then the with widnow function offered higher performances than those without the window function. In this regard, it was found that the with window function has acheived a maximum packet reception rate than that for the without window function for different tunable parameters. In relation to the power consumption scenario, it was determined that the without window fuction proved to produce energy saving performances than the with window function. There are several interesting aspects of the transmit power control mechanisms highlighted in the results and discussion chapter.

***Keywords*:** TPCM, ExNode, FPGA, WARP Board, ACK, RSSI, ExMAC, PRR , SISO, QoS, TDMA, RTP.

ACKNOWLEDGEMENTS

This thesis research work was successfully conducted at the Wireless Access Network (WAN) of Ericsson Research, Kista in Stockholm, Sweden. First of all, I would like to express my sincere graitude to my supervisor Vicknesan Ayadurai for his understanding, patience and personal attention. I am also extremely indebted to him for his highly supportive guidance and encouragement throughout the thesis, I am really proud to have him as a supervisor.

I am extremely thankful to my project manager Mikael Prytz, for his continuous support and providing the necessary resources to accomplish my thesis research work. I am very much thankful to him for choosing me as a thesis student at Ericsson Research, Kista, Stockholm.

I would like to express my greatful and sincere thanks to my supervisor, Johan siden at Mid Sweden University, who has given outstanding support and guidance for my projects and thesis work.

I am very thankful to Prof. Bengt Oelmann for his understanding, support and for also giving me such encouragement to complete my master's thesis work at Ericsson Research.

I would also thank to Gabor Fodor for his guidance and suggestions on my work.

I take this opportunity to thank my colleague and a great friend Fatou Ndiaye from KTH university, for her valuable discussions, good support and always finding a great time to have discussions with me.

I owe this life to my parents and also to my brother, Balachandra Reddy Kandukuri, who has given constant encouragement and guidance through out my life and it is only beacuase of him that I am here.

Finally, and most importantly I would like to thank my friends for their constant support and encouragement.

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TERMINOLOGY / NOTATION

Acronyms / Abbreviations

- **ACK** | Acknowledgement.
- **CIR** | Carrier-to-Interference Ratio.
- **DST** | Destination.
- **ExNode** | ExMAC WARP Node.
- **FPGA** | Field Programmable Gate Array.
- **MAC** | Medium Access Control.
- **MIMO** | Multiple Input Multiple Output.
- **PRR** | Packet Reception Rate.
- **QoS** | Quality of Services.
- **RSSI** | Received Signal Strength Indicator.
- **RTP** | Real-time Transport Protocol.
- **SISO** | Single Input Signle Output.
- **SN** | Sequence Number.
- **SRC** | Source.
- **TDMA** | Time Division Multiple Access.
- **TPCM** | Transmit Power Control Mechanism.
- **WARP** | Wireless Open-Access Research Platform.
- **Xilinx EDK/SDK** | Xilinx Embedded Development Kit/ Software Development Kit.

INTRODUCTION

Power control plays a prominent role in communication systems for both uplink (mobile to base station) and downlink (base station to mobile) communication channels, in order to accomplish control with regards to the power levels of the Quality of services (QoS) system. The QoS of a communication system is a set of parameters which must be fulfilled by the operator and these consist of the bit error rate (BER), packet error rate (PER), packet delay, SIR(signal-to-interference ratio), noise and RSSI (Received Signal Strength Indicator) and so on. The majority of the previous power control methods have been implemented in simulation setups by using the mathematical proof-of-concepts. For some cases these simulation setups may not be as successful in real networks or devices because less consideration is given to QoS. In this thesis work, consideration has been given to the design and development of new prototype power control alorithms on WARP testbeds for any pair of nodes or devices. Its main focus has been to acheive high packet reception rate, lower packet loss rates, low power consumption and better RSSI performances.

In this thesis, a new transmit power control mechanisms on WARP boards for point-to-point communication systems, is being introduced into this research laboratory. In this case, the power control mechanism is only being operated on transmitter side. This mechanism has been designed and implemented using system C programming in addition to the existing code in accordance with the Xilinx Software/Embedded development tool kits. The measurement setups have been completely built and developed in the WARP nodes, environment, which have been implemented so as to consider the system QoS requirements such as the avoidance of packet losses, a reduction in traffic between the base station and the devices, an increase in node capacity and to reduce the power consumption.

This thesis work focuses on two main tasks namely, the theoretical investigation into the background for power control concepts and any related work and, additionally it will explore the background in relation to communication systems together with power control. It will also explain how power control systems work in real world applications and the environmental challenges that could be faced and there is also sub-category within this chapter which is a literature survey, which deals with power control management systems and their applications, and also to the related work regarding the proposed power control mechanisms. The second investigation focuses on new prototype transmitter power control mechanisms for FPGA WARP boards and this is also sub-categorized into two sections, existed hawrdware and the software setup of WARP boards and the other part focuses on the reconfigured hardware development structure of WARP nodes. In this work, a simple feedback concept has been proposed which is based on transmit power control mechanisms on WARP boards for a node to node communication system and in which the operating frequency of WARP node is 5GHz. The following sections 1.1), 1.2) and 1.3) present the thesis goals, the scope and an overview of the report.

1.1 Thesis Goals

The following is a list of the goals:

1. Propose a new prototype method of Transmit Power control mechanisms.
2. System design and implementation of transmit power control mechanisms on WARP boards.
3. TPCM Measurement setups on Boards.
4. Results and comparisons between two proposed and developed mechanisms.
5. Conclusions and Future work

1.2 Scope

Because of the time constraints placed on the thesis its scope has been limited to a choice of two non-formula based prototype transmit power control mechanisms and to design and develop them based on the feedback ACK concepts from the receiver node. This setup has been measured on a WARP boards environment. The targets are to reduce the packet losses, packet latencies and to also improve the system efficiency.

1.3 Organization of Report

The organization of the report is as follows,
Chapter 2: Provides a discussion for the literature survey relating to on previous concepts of different power control mechanisms with consideration to the its advantages and disadvantages.
Chapter 3: Explores the background in relation to WARP boards and their features such as radio boards, clock boards and antenna features.
Chapter 4: Represents the proposed methods of transmit power control structures and the system designs for the mechanisms which have been developed in C. In this section, the implementation of the results which were observed from the controller PC measurement setup of WARP boards are given.
Chapter 5: Describes the results, discussions and its applications followed by the conclusion.
Chapter 6: Based on the proposed and developed mechanisms from the results, suggestions for future work are offered.

Background and Related Work

Communication systems have faced serious environmental challenges under different circumstances including major impact from CIR, multi-channel interference, vast temperature ranges and high power consumptions. This interference occurs when users are sharing the same communication channel link or from a lack of separation between the users, for both up/down link channels. However, it is the uplink channel interference which proves to be more serious than the downlink channel communication. Mobile stations signals are always moving at different distances with respect to the speed of different fades before reaching the base stations. Unlike mobile stations, base station signals are travelling with similar fades before reaching the mobile stations. The base station transmitter could be capable of transmitting stronger signals, which would then mean that the signal will be transmitting very quickly. In this case, the power control should be faster than the fading; otherwise, it will not be to control the power levels. When the power control algorithms are achieved for controlling the system QoS requirements, it will still prove easier to estimate the performance levels of power control algorithms effectiveness and its convergence speed.

In particular, in general applications, multi path fading describing the channel links between transmitter and receiver is stochastic in nature, and the mobile terminals are always moving at various speeds and thus the channel fades are not predictable and the propagation effects involved are refraction, reflection, scattering and shadowing. Signals reflects from smooth surface and when the signals encounter sharp edges of buildings, they will then refract, while a rough surface will scatter them. When the signals are blocked by buildings and walls, then they pass through them thus causing shadowing. All these effects cause the channel to be lognormal, Rayleigh and/or rician, in this case both are distributed. The figure below represents the transmission of signals which travel in different paths to the receiver. A general view of multi-path fading is shown in figure 2.1.

The receiver receives the same signal multiple times with respect to different times and phases. These signals are added either constructively or destructively based on the phase signals. The radio signal undergoes a path loss, which depends on the signal travelling distance between the transmitter and receiver. The exponent of a path loss ranges from 2 to 5. Fading is the attenuation of propagating waves during its time interval. Fading can be categorized into two types, namely fast or multi-path fading and slow or shadow fading. Mainly, shadowing effects are caused by buildings, mountains and stages etc. The best examples of multi-path fading are, for Single-inputs-Multiple outputs (SIMO), Multiple-inputs-Multiple outputs (MIMO).

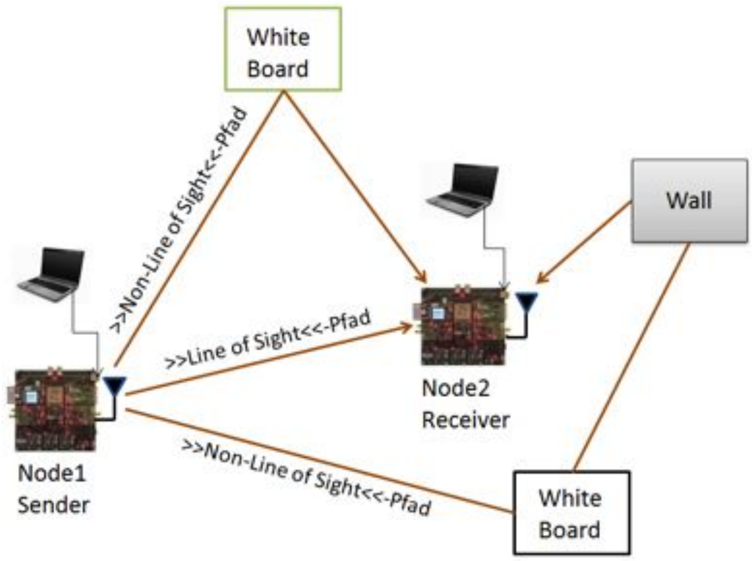

Figure 2.1: Intereference of Mutli path Fading.

2.1 Power Control

The main objective of power control is to obtain a better signal-to-interference ratio, which meets the signal QoS (Quality of service) requirements for the node. The power control serves to adjust the power levels based on the application requirements and there are multiple means of adjusting the power levels by following the indoor and outdoor environmental challenges.There are two categories for power control

1. Inner loop Power control
2. Outer loop power control

Inner loop power control system a sub-categorized into two parts namely open loop power control and closed loop power control. The open loop power is used to solve the near-far field effects and shadowing problems. In order to achieve this the method will monitor dynamically and the node will adjust its transmitting power. The node will estimate the signal strength of the transmitter by measuring the received power level of a pilot signal from the network to the mobile and is able to adjust its transmitter power levels, and there is no feedback concept. A closed loop power control describes the transmission of the signal from the mobile to the base station, which means the uplink transmission. It can adjust the transmitted power levels by receiving a feedback response from the base station and the performance is better than that for the open loop power control and it is slower to change its channel behavior. It works for both uplink and downlink transmissions and prevents fast-fading effects. It is also known as fast closed power control and this technique is used for both uplink and downlink transmissions. Based on the QoS requirements, the outer loop power control will be maintained at the correct CIR levels and it calculates the frame error rate (FER) by varying the energy per bit to the noise power spectral density (Eb/No) which will meet the desired FER. In general, both open and closed loop power controls have been used to provide better system performances.

2.2 Related Work

This section explores the properties and applications of different power control algorithms and their features. Previously, many authors had conducted their investigations into power control applications for different communication systems using cellular and mobile broadband communications, wireless networks and Wi-Fi and so on. Throughout the survey, the focus was on published journals and conferences papers of power control algorithms since the 1990s to 2010. PCAs had been proposed and developed for the predefined and advanced communication systems including the GSM, CDMA, WCDMA, 3GPP and LTE networks. In the field of power control management system, centralized power control algorithms describing the fact that the constant Carrier-to-Interference ratio is maintained for all the receivers, were proposed and proved [6]. However, CPC is complex to implement for many applications, as it requires a significant amount of bandwidth, and references to design and the implementation of distributed power control algorithms. However, it is feasible to implement it for many communication systems and it is easy to maintain and cheaper than the Centralized PCAs. From the previous research papers, the results were explained and discussions of PCA's had been presented in this chapter. However, beacause of the limited scope of the theis, many interesting topics have not been dealt with. The focus of the following sections is on selected research papers involving power control mechanisms and their features for the corresponding work.

2.3 Literature Survey

In this section, convergence speed is an important criterion in relation to power control algorithms and together with the distribution, they should be capable of working in an aggressive manner and thus achieving a distributive convergence of the system. This occurs when there a maximum number of possible users. Power control methods in communication systems pay significant attention to Zanders researched and published papers on centralized and de-centralized or distributed algorithms, constant CIR (carrier-to-interference ratio) balancing. Further investigations of CIR balancing have been performed by Grandhi et al [6]. Foschini and Miljanic its more realistic model in relation to positive receiver noise and target CIR [11]. This FCA mechanism was stated to converge its speed either synchronously or asynchronously for the fixed point of a feasible system and based on this Grandhi et al proposed and extended the framework of upper link transmission power control [7], which is also called the Distributed Constrained Power Control (DCPC). Device-to-Device communications for the cellular infrastructures have been proposed and stated from a distributed power control and a mode selection algorithm by Norbert and Gabor [12]. It describes the near optimum performance for both single-input-multiple-output (SIMO) and multiple-input-multiple-output (MIMO) communication settings [12]. The mathematical proof of concepts has been involved in the power control, some of the parameters, assumptions and terminologies follow represented number of base stations N and number of mobile stations M in the system for the power transmitted by the mobiles as P= [P1, P2... Pm] as well asCIR at the mobiles. The gain matrix G is represented as a base station i communicating with mobile station j, given by Gij. All the links are represented between each and every base and mobile stations. This mainly focus of this paper on MIMO communication link services for advanced cellular infrastructures, there are many proofs and problem definitions were highlighted in the implementation and results sections at [12].

2.3.1 Centralized Power Control

This section focuses on a centralized power control management system which operates the power levels by means of a central controller. This central controller has the correct information with regards to all the radio links in the system. This is complex to implement and assists in the design and development of distributed power control schemes. This mechanism was proposed and proved by Grandhi et al [6] and it was used to develop a distributed power control scheme [16]. In this paper, main focus was on developing the same optimal solution as from [16], [17]. In this case, [7] they considered the same idea as put forward in, which is also applicable for the dowlink side (from base to mobile). This scheme can compute the transmit power which directly effects the CIR, which means that every mobile station for the transmit power will adjust its CIR to a normal value. It uses the global information by updating the powers and balancing the CIR. The CPCA also reduces the mathematical problem so that it is possible to compute an optimum vector. The corresponding complete CPCA CIR balancing proofs, problem definition and analysis are described in [6].

2.3.2 Distributed Power Control Management Systems

This distributed power control management system uses only local information for monitoring the powers and CIR balancing. Many distributed power control schemes have been described for different applications QoS requirements. DPCs are iterative and they converge to the desired value after a particular number of iterations. The number of interations involved determines the responsiveness of the algorithm. There are different types of distributed algorithms which have deen developed with different properties of communication systems such as TDMA, FDMA, CDMA and WCDMA and so on.

2.3.2.1 Distributed power control Algorithm (DPCA)

This is the initiator of the distributed power control schemes and it was developed and it updated the settings for many communication systems such as satellite communication systems, after that it was enhanced for cellular communication systems. The convergence speed depends on the C value, which was derived in [7]. It converges to the optimal CIR. The main disadvantage of the DPCA is that it is not fully distributed, because DPCA requirements for some global information are determining the normalization constant C [7].

2.3.2.2 Fully Distributed power control Algorithm (FDPCA)

FDPCA uses only local link information and does not work for global information in relation to the control of the powers and offers better performances for cellular communication systems. There are many interesting aspects of algorithm proofs and results have been described in [10]. The main disadvantage of this algorithm is that n tends to infinity the power p tends to 0. The power levels of all mobile stations tend to zero. In addition, the extension of FDPCA was described and proved as an Improved fully distributed power control (IFDPCA) algorithm, this is the extension of FDPCA. The difference between these two algorithms explores the minimum value of the CIRs and maximum value of CIRs and the expression can be seen in [14].

2.3.2.3 Balanced Distributed power control Algorithm

This mechanism was proposed and proved by Wang et al [14] for CDMA systems. It describes the balancing of the power levels by adding both FDPCA and IFDPCA. This means that the power goes neither to infinity nor to zero. This algorithm works for both up and down link channels in order to balance the power levels of the transmitter and receiver. If it crosses the uplink channel, then the FDPCA can be applied, if it crosses the downlink channel, then the IFDPCA will be applied.

2.3.2.4 Distributed Fixed Step power control Algorithm (DFSPCA)

This algorithm was proposed and proved by Sung et al [4], and is a simple feedback power control algorithm, which describes many useful properties such as link quality and bandwidth efficiency etc. The existence and proposed power vectors proof of concepts were given in [4]. DFSPCA was described, based on the CIR received and it has a window function for comparing the received CIR. In this case, power levels were operated using only two commands, which means power up command will apply when the received CIR is below the window. If this is not the case, then the power down command will be sent, when the received CIR is above the window, or, if it goes within the window, the power levels will be the same. This is called a bandwidth efficient algorithm since it uses only two bits for controlling the power. The disadvantage of the algorithm, when the QoS requirements are restricted, is that the system capacity decreases drastically.

2.3.2.5 A Feedback Based Power Control Algorithm Design for VANETs

This feedback approach algorithm was proposed and developed by Xu Guan et al [3], and this research experiment was conducted in the simulation setups of vehicle-to-vehicle broadcast communication in vehicular adhoc networks. The authors were developing the power control mechanism based on the feedback approach to the receiver, and the FBPCA was designed and developed for the vehicular adhoc networks, such as vehicle-to-vehicle communication. This was tested for a particular targeted communication range, using the GPS communication system of the vehicles. In this case, they designed the packet structure by following the properties of Node ID, position data, target range, Feedback Beacon and payload. This algorithm was mainly designed for use in higher communications reliability by reducing the collisions for safety communications and the conclusion was that the power control algorithm has the ability to reduce the transmission power significantly in order to achieve a higher packet reception rate than without the power control algorithm and the results were discussed and can be found in [3].

OVERVIEW OF WARP NODES

3.1 Existed FPGA WARP Hardware

The Wireless Open-Access Research Platform (WARP) is described as ”a scalable and extensible programmable wireless platform, built up from the scratch, for the advance prototype wireless networks” [1]. In addition, WARP can be expressed in brief as a C programmable interrupt driven embedded system. The ongoing research and development of WARP by Rice University and several research industries also working on WARP (Ericsson Research, Xilinx, Nokia Siemens Networks, and Motorola Research) also invovled work by the research universities (University of California, San Diego; University of California, Irvine; WINLAB at Rutgers University) who were also using the WARP test platform [1]. The WARP project has two important goals. The first one is in relation to open-access research, since so far the commercial chipsets based on the IEEE 802.11 WLAN standard had been locked. It thus enabled the WARP hardware and software, required for the research into the next generation of wireless networks to be used. The open-access research involved a community of researchers who pool their different aspects so as to create new prototype wireless networks [1]. The second goal was to place ”the wireless in wireless curricula”, which means that both academics and research students would be able to perform ”hands-on” wireless real time (WARP Workshop) and non-real time (WARPLab) communications [1].

3.1.1 FPGA WARP Board

Instead of microcontrollers, the WARP test node platform used Xilinxs Virtex II Pro FPGA for processing and storage [2]. The FPGA WARP board supports up to four daughtercard slots. The FPGA board specifications can be described as a 4Mbytes Onboard SRAM as the instructions and/or data memory. For the external I/O ports, WARP has a serial port for basic input/output to/from FPGAs embedded processors, an ethernet port for the MAC layer implemented in FPGA and multi-gigabit transceivers for inter-board communication for multi-FPGA processing. In figure 3.1 the FPGA board is whown and the WARP provides daughtercard connectors from which some expanded functionality can be realized. It supports radios, video cards, A/D and D/A cards, and also detailed specifications can be seen in figure 3.1 below.

Figure 3.1: General view of WARP Board

The following figure represents the development process of the FPGA. The hardware designs for the FPGA signal processing are built in Sysgen software (SW) and implemented in C code which is operating for the integrated PowerPC processors.

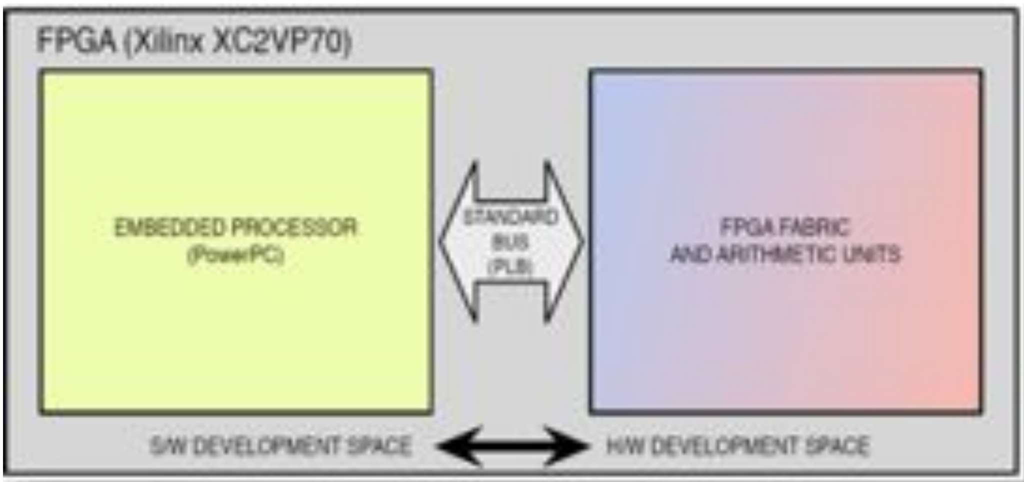

Figure 3.2: General architectural view of FPGA

3.1.2 Radio Board

The radio boards are using a WARP board Maxims Single-/Dual-Band 802.11 a/b/g World-Band Transceiver chipset. The operating frequencies of the radio board can be set to operate at either 2.4 GHz or 5 GHz with 40 MHz of bandwidth, According to our own wireless node protocol stack, the operating frequency is 5GHz and the detailed specifications of radio board can be seen in figure 3.3 and it is also aligned in a single WARP FPGA board, which is able to place up to four daughtercards. This means that the WARP boards are embedded with four radio daughtercards, which enables the use of MIMO techniques, testing and verification. In practice, the testing of MIMO technology is crucial, since it is the technology being used for the 4th Generation (4G) of mobile and broadband communications.

Figure 3.3: General view of Radio Board

3.1.3 Clock Board

Figure 3.4: General view of Clock Board

This clock board provides the clock signals for all parts of the WARP board and it has two sections, the first giving the reference clocks for the radio boards and the second for the FPGA logic and analog converters. Both have the option of accepting their clock inputs from an on-board temperature compensated crystal oscillator or through an off-board connector. The next option allows for multiple warp boards to share common clocks for beam forming or for multi FPGA applications and the board specifications are represented in figure 3.4.

3.2 Reconfigured WARP Hardware

In this setup, Ericsson Research and University of California collaborated to construct the newly added system hardware components, design and for which the development was conducted by the University of California, San Diego. It was designed and developed for the ongoing research regarding Ericsson's requirements and the implemented hardware components added in the configurable region of FPGA WARP board were the SISO TXRX PCORE developed by UCSD and TEMAC developed by Xilinx (temac) and the software setup has been implemented by Ericsson research. The FPGA WARP board has contained two hardware regions, first involving the fixed hardware components and as CPU, IC, DMAC, MEM, Data and control buses. In this region, it is not possible to change or add any hardware components, and the second deals with the configurable hardware region. It is possible to conduct the new hardware design and implementation based on the work requirements

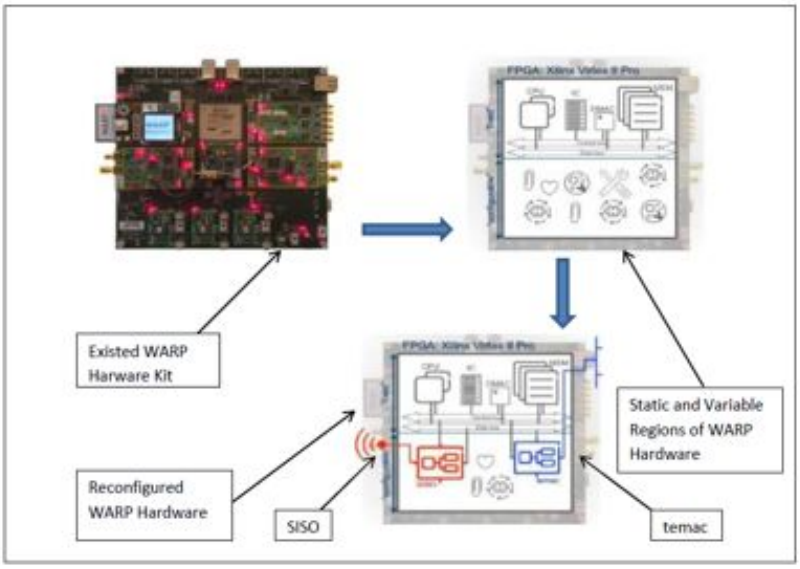

Figure 3.5: General view of Reconfigured WARP Board

3.2.1 Wireless Node and Protocol Stack

This protocol stack is an implementation of a networking protocol suite. The wireless node is referred to as the WARP node together the master PC provide for the continuous packet transmission over-the-air. The master PC contains free BSD OS and higher datacom layers and the WARP board contains its own-code plus hardware and lower radio layers. This entire structure is referred to as Ericsson research's own protocol stack. It contains several layers of OSI such as application, transport, network, data link, MAC and physical layers. In order to extend it, WARP drive provides the communication link between master PC and the board. It provides the transmission of real packets over-the-air through omni-directional antennas and a description of the antenna is given in the section below.

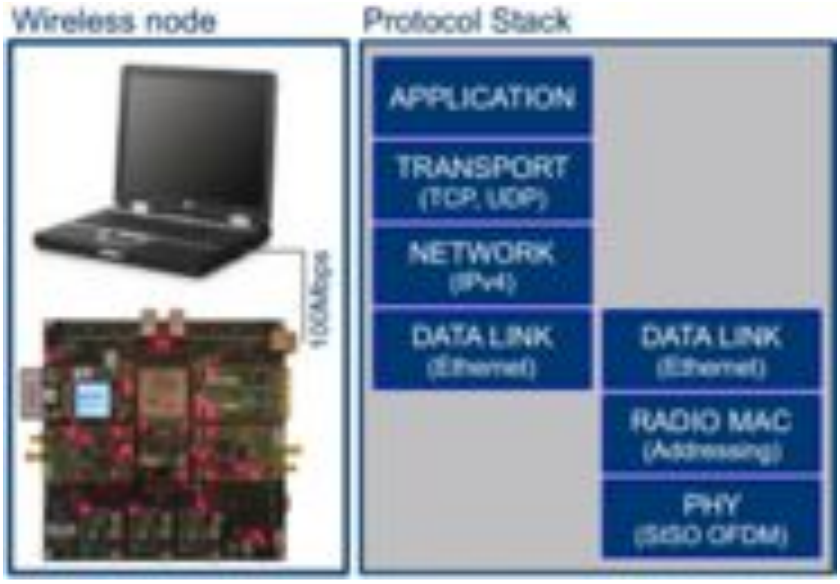

Figure 3.6: Wireless ExNode with Protocol Stack

3.2.2 Omni Directional Antenna and Features

The omni directional antenna, which radiates power in all directions at one plane for wireless communication, is widely used for radio broadcasting, such as mobile devices, wireless access networks, FM radios, GPS, cordless phones and base stations etc. and thus serves many communication devices. It allows many applications to overcome interference but it also leads to directional waste of power. This was proved when, devices are communicating with a single mobile user or device, for instance network infrastructure such as cellular and WLANs. The given figure below shows the omni directional antenna of the WARP boards.

Figure 3.7: ExNodes Omnidirectional Antenna

3.2.3 WARP Testing

WARP functions as a wireless bridge between computers and therefore it has many output/input ports. First of all, the Universal Serial Bus (USB) is used to transfer the codes which were created using the Xilinxs platform studio from the computer to the FPGA. The ethernet ports are used to create the sink and the source between the connected computers. When a computer has a packet which it sends to another computer, it will use the Ethernet connection to transfer the packet to the WARP node, which then sends it wirelessly to another WARP node (destination). Upon reception of the packet from the air interface, the other board uses the ethernet connection to transfer the received packet to the source computer.

SYSTEM DESIGN AND IMPLEMENTATION

This proposed power control mechansims were investigated in the literature survey, and reseacrh papers have been discussed in chapter2. The main ones considered were "A Feedback-based power control algorithm design for VANET" by X. Guan et al [3] and "A Distributed fixed step power control algorithm with quantization and active link quality protection" by Sung et al[4]. [3],[4] proposed and proved simple feedback adjustment alogrithms using simple metrics for vehicular communications (VANETs) and cellular communications have also been represented in [3], [4]. The decision was thus taken to follow the basic ideas of feedback approach in [3] and [4].In addition, a new proposal of non-formula based feedback power control mechanism is being introduced here and in order to test and verify it in real environmental conditions using WARP boards for the point-to-point communications, the followings sections articulates the system design and implementation of TPCM.

4.1 ExMAC Header

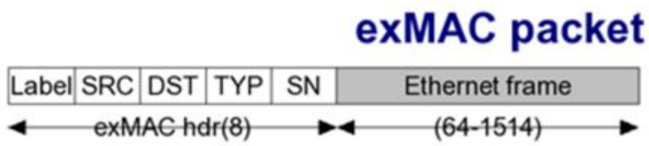

Figure 4.1: Genereal structure of ExMAC Packet

Exmac addresses eight fields of the header size and every field has its own specific names such as Label, which addresses fields zero to three and for which every field of label contains 8-bits. Source (SRC) is an 8-bit addressing field and it is used to find the SYNC to the destination node, which means where-to-where. Destination (DST) also contains 8-bit addresses and it specifies the destination of the packet, i.e. where to receive. Type (TYPE) represents the 8-bit field including a clone bit, and it indicates the packet type regarding whether it is data or ACK or something else. Field of the sequence number (SN) addresses the 8-bit MAC sequence number providing the unique identification of every packet sequence and the overall structure of the fields referred to as the ExMAC packet.

4.2 Design Flow of TPCM

This transmit power control mechanism is illustrated in a flowchart shown in figure 4.2. It was designed and developed from the basic idea of a feedback based power control algorithm for VANETs [3] and a distributed fixed step power control algorithm [4]. The main purpose of the power control is to check whether the nodes have continuous communication channel connectivty or not, which means without any packet losses. In this case, both nodes have transceivers, so as to check their connectivity due to the interference or packet losses.

This section focuses on a description of the design flow for the transmit power control mechanism for point-to-point communications. In the earlier version, there is no power control management system for the FPGA WARP boards for node-to-node communication. According to the Ericsson research requirements, the proposal is to design and develop new power control mechanisms. The design structure below is the point-to-point communication between two WARP nodes, namely Node1 (transmitter) and Beacon Node2 (receiver or base station). The first design flow graph explores the operation of the transmit power control mechanism, how it works, where to send and obtain the packets and this always in association only with the transmitter node. It also shows who sends the data packets to the receiver. The second part describes the loop iteration of the power control management system, which means how the power mechanism will work together with the transmitter node and it also shows the detailed information of the loop iteration operations. The reason for this is to consider the design of the packet window function.

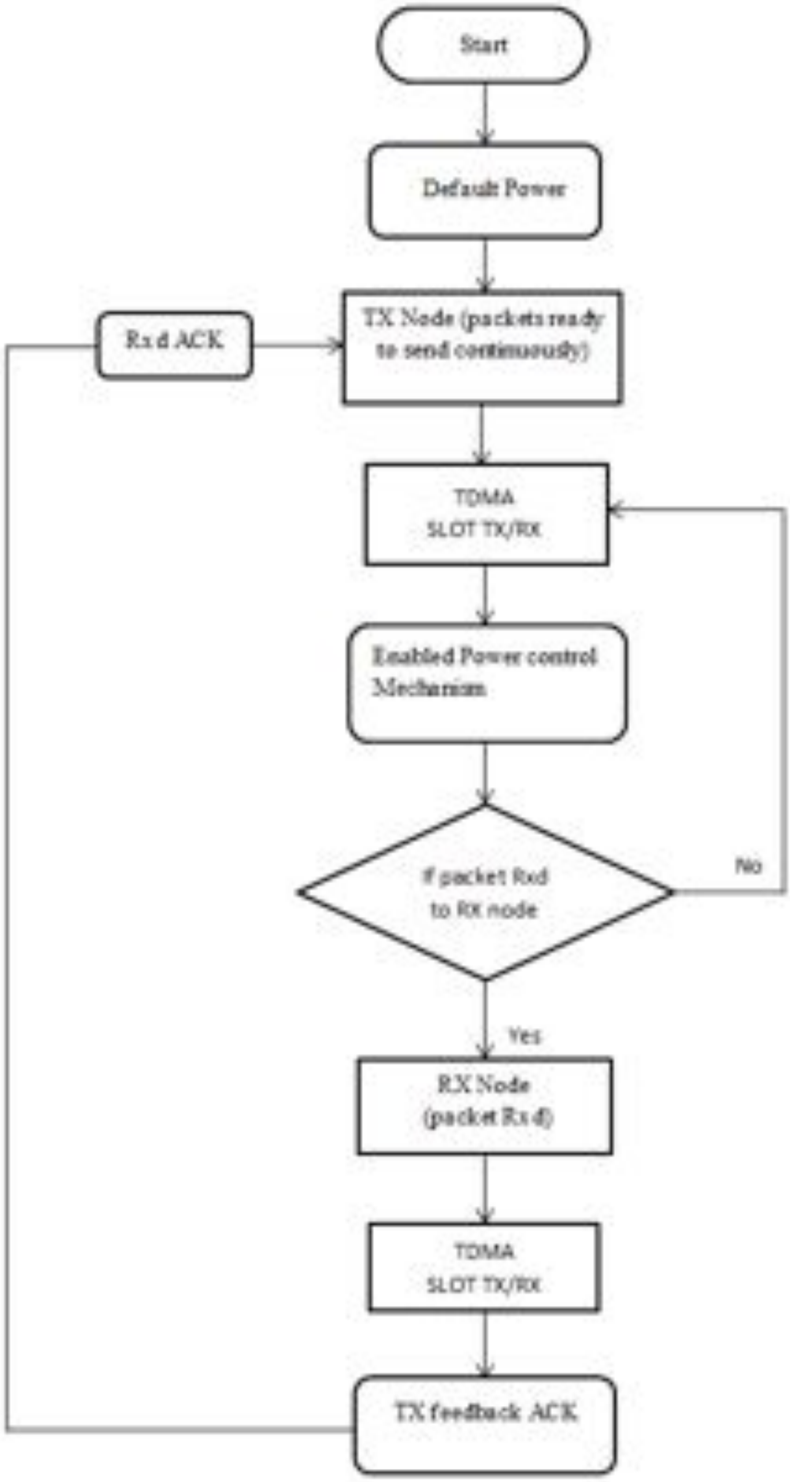

Figure 4.2: Flow graph of Exnodes along with TPCM

4.2.1 Transmit Power Control Mechanism with Window Function

In this section, the focus is on designing the transmit power control mechanism with the window function. The main consideration for this property is to achieve high packet reception rate at lower power levels. The packet window size will vary depending on the system requirements and the performances with regards to this property are clearly stated in the results and discussions chapter. This packet window function array addresses the losses and no losses. The main purpose of the packet window function property has been considered in order to determine the exact packet losses, while the nodes communicate with each other, as they sometimes are used to deliver dummy packet losses due to errors of the upper or lower protocol layers or based on intereferences whether it is an indoor or outdoor environment. In this case, every data packet will carry out the data only by means of the window function, if the packet does not arrive successfully to the receiver, then it will be able to find the packet loss using the current TX packet sequence number. Following this, the packet window function will obtain the current transmitted data packet loss sequence number with reference of the repeated last ACK sequence number, thus it will be differentiated by the means of the last feedback ACK sequence number of the receiver and if the last ACK sequence number has a difference of 1 from the current TX packet sequence, that means that the packet has been either sucessfully received or has been lost.

The TPCM node which has been sending the continuous data packets to the receiver node (Beacon Node), while receiving the packets, will be processed in order to send the feedback acknowledgement (ACK) to the transmitter power control node. The design flow goes through the step-by-step process of the TPCM and for each step of the process, there are alternate processes and decisions that are co-related to each other. First of all, several tested designs of the power control mechanisms have been made and finally, there was the introduction of the packet loss window concept in order to avoid the losses until the power threshold. The window size considered was to design five or more packets of the data with sequence numbers, while transmitting the data packets to the window function which will count the number of packet errors as well as the number of successfully received packets (which means no losses). Whenever the packets are received by the receiver node and the receiver will then send the feedback ACK to the transmitter node. If the packet does not arrive successfully to the receiver this means that the packet loss occured at the transmitter node, thus the power control will increase the power level for the next packet transmission. Every packet of the transaction window function will be updated and serve with new results whether the window has losses or not. In addition, using the counter function, packet losses will be calculated from the window function. When Beacon Node2 receives the packets, then it will send the feedback ACK to Node1 meaning that it is delivering the successful transmission of data packet. If the packet is not received, then the counter will be counted for the packet losses by using window function. If the packet loss counter found the packet losses from the packet window function to be more than two continuous packet losses and the power level to be greater than 63, then the power control mechanism will send the Power Up request to set the new power level in order to reduce the losses until a steady state power threshold is achieved. If the packet reception rate is high, then the packet losses are zero and the transmitter node will apply the request to power down based on a given number of successfull data packet reception of the receiver as being 5, 10, 25 or 50 or more as well as when the power is greater than zero. Then the power control mechanism will be reducing the power levels until a steady state power threshold has been achieved and thus increases the node capacity. When the system runs, the iteration of the power loop will be performing continuously by considering many circumstances, such as interference, Line of Sight (LOS) and Non-line of sight (NLOS). The other interesting aspect of power control mechanism is that the power levels operated only on the transmitter side and this is also known as the transmit power control mechanism (TPCM). Its performance is based on the TDMA slot system and it works according to the simple feedback ACK principle.

Figure 4.3: Flow graph of Transmit Power control mechanism with window function

4.2.2 Transmit Power Control Mechanism without Window Function

In this case, the packet window funtion property was not being considered and the remainder of the design structure is almost same as that for the with packet window function. The main aim of introducing this concept is to the performance evaluation in relation with and without the packet window functions for the transmit power control mechanisms.

The flow graph of the transmit power control mechanism without the window function give the detailed specifications, differences and performances between with and without window functions. This flow structure helps us to develop the transmit power control mechanism without window function and by using this it is possible to analyze, how rapidly it converged to the steady state threshold region as well as determining how much energy it cosumes and also the packet losses which occured during the continuous packet transmission. These two power control loop designs will be referred to determine the performance evalution of the power control mechanims thus being able to determine which are faster and which are more aggressive, while also saving power and reducing the packet losses.

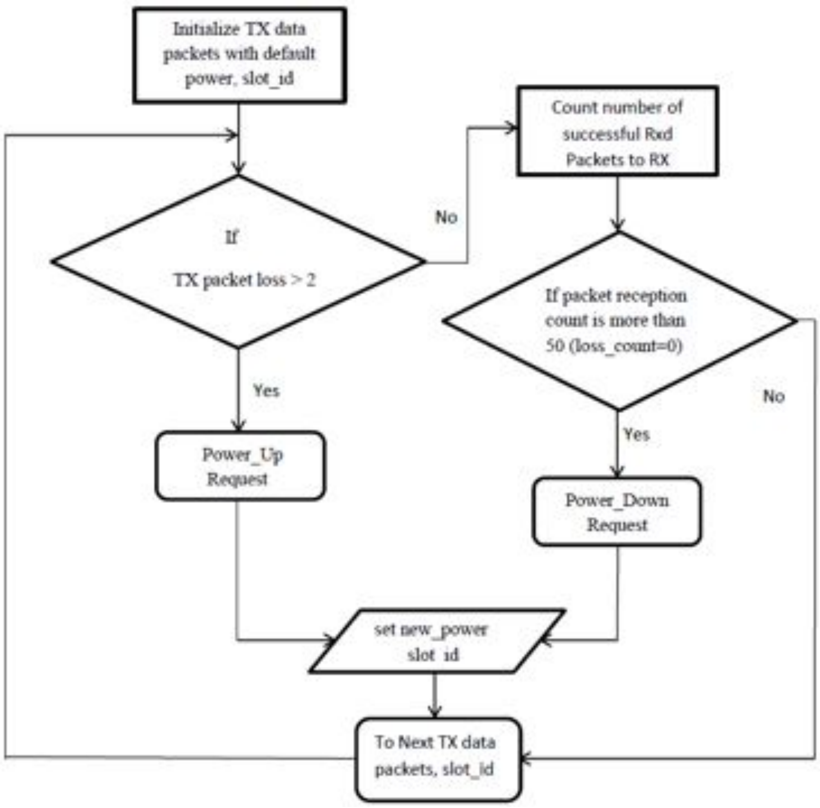

Figure 4.4: Flow graph of Transmit Power control mechanism Without Window Function

4.3 Implementation of Transmit Power control Mechanism

This section follows the step-by-step procedure of implementation shown below. It offers a brief description of the implementation and explains how the WARP nodes are communicating with each other over-the-air.

1. To develop the C-code in accordance with the WARP repository recommended tools by Xinilx Platform Studio.
2. Require to test, verify and debug the code.
3. To download the code on WARP Nodes through USB (Universal Serial Bus) cable
4. Wireless Node (WARP) with Master PC access via PuTTY SSH from PC controller
5. After downloading the code, using warp-drive terminal to communicate with WARP Node, as seen in the Appendix.
6. With the assistance of the TDMA system to transmit or receive the packets via ten slots (Slot-ID, Slot-TX, Slot-RX) on the warp-drive console.
7. Radio board of omni-directional antenna serves to transmit or receive the packets over-the-air.
8. RTP SRC commands to assist in the setting of the parameters on console terminals.

The above given system design flow graphs were referred to in order to develop transmit power control algorithms for the transmitter node. First of all, the required data functions within the power control loop were intialized and seperate source and header files were created within the power control project, then conditional statements for enabling the power control in the main source file were set, in order to access all the information through the main file and then into the power control source file. Several steps were involved in order to iterate the power control and all of the structures, functions and variables are working together.

The power control mechanism has been implemented by following a set of variables for the system design structures. First of all, the mechanisms were implemented and tested for point-to-point communication using FPGA WARP nodes. In this laboratory, there are four different testbeds or nodes to test and verify the codes together with the power control to adjust the power levels automatically. However, no power control management systems exist in this laboratory. In the reference to the case study and analysis, simple feedback transmitted power control mechanisms on WARP nodes have been proposed. The main goal of the power control has been developed to prevent the data packet losses on the transmitter node and to increase the system efficiency. The following measurement setups are performed by any pair of WARP nodes, one being the transmitter node, which will send the data packets to the receiver and the other is the receiver node which provides the feedback ACKs for every successful transmission of the message signal. In this scenario, the transmitter node does not have any delay functions to wait for the feedback for a successfully transmitted signal and thetransmitter node always sends the data packets continuously without considering the losses thus making it unnecessary to consider Ready, Listen and Idle state modes on the transmitter side. According to this protocol stack, continuous data transmission is always being considered. In this development process, prototype concepts for

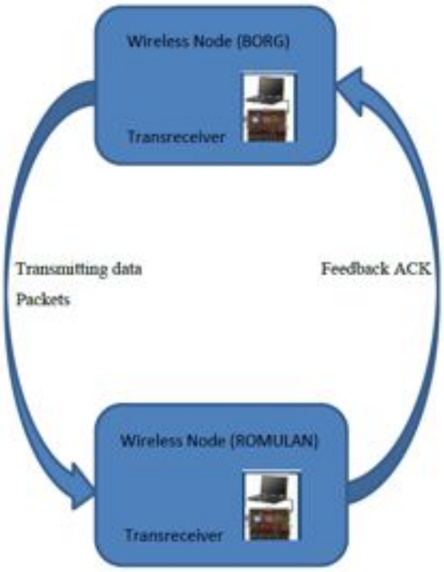

Figure 4.5: Flow Design of Exnodes

Xilinx Software/Embedded development tool kits were conducted in accordance with the WARP repositories provided by Rice university, and also the previous projects, implementation has been developed in the Xinilix SDK/EDK tool kits. The power control implementation has followed to work together with previous project source files. In this implementation, several parameters for board environmental challenges have been considered such as intereference, losses and RSSI. In order to obtain the above challenges, three conditions has been set, namely, to adjust the power levels as power-up, power-down and default power.

Power control implementation is a process used to develop the ability of the data packets over-the-air with respect to the power levels, regarding continuous data packet transmission which requires an overall controller regardless of whether the data has been successfully received or not and how many packets were received or lost, whether the successfully received packet sequence numbers were matched with the feedback receiver sequence numbers or not. In this implementation, two main considerations

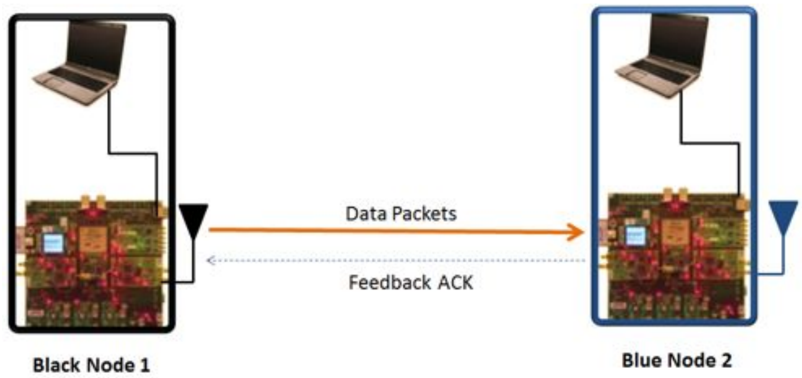

Figure 4.6: Point-to-Point Communication of Exnodes along with TPCM

were developed namely, with and without window function properties. According to the window function property, this maintains the continuous data transmission packet and feedback packet sequence numbers in the window function for calculating the losses or no losses from a given number of packet sequences and this function mainly works with First-In-Last-Out (FILO) concept. The complete packet transmission data is stored in the packet window array function, updated and monitored on the transmitter power control loop iteration, which means how many packets were received successfully and how great the losses will be. This type of investigation has been performed on the window funtion. It will assist in making decisions with regards to the power level and which power state will be required to be changed for the next data packet transmission. It is not possible to make a decision with regards to the threshold power based on a single packet successful transmission as the threshold will constantly vary and by introducing the packet window concept, it was possible to determine the correct threshold region. It will then be possible to decide to make a change based on losses or no losses until a steady state power from the upper or lower region of the threshold. The packet window funtion assists in the operation of the power levels as to whether it will use for a power up or power down or power now request.

The complete control process is operated by the TPCM and if the window function has losses, then the transmitter power control node increases the power up until the steady state power threshold region is achieved. If the packet loss rate is equal to zero based on the continuous packet transmission, then the power will automatically be ramped down until the threshold region is achieved. The power control mechanism should be always monitored in order to obtain the received signal strength at the power threshold region and in this case the operated power level of the receiver node is the default option. In the worst environmental circumstances, if it is required to change the power levels in order to achieve a better signal strength, then it is also possible to manually change the power on both sides.

In this implemetation, the data was transmitted or received through the TDMA slots. TDMA stands or time division multiple accesses and it is a channel access method for sharing the medium. It allows several user nodes to share the same frequency channel with different time slots. TDMA based system contains ten slots to perform both uplink and downlink channel access. According to the power control mechanisms, the TDMA system has been developed for the exNodes communication with each other. It involves the sharing of the information through slotid, slottx and slotrx. Slotid represents the name of the all slots from slot0 to slot9, where the slot0 is a beacon slot and the node transmission and reception process will always start from slot1 to slot9. In addition, the data packet and received packet information is being delivered on RTP SRC terminals by means of SSH PuTTY console terminals. These are two types in which one side is showing the information for ether packet transmission and the other side represents ExMAC packet transmission or reception data. The entire packet transmission and reception processing through real-time transport protocol (rtp) source is by means of the transport layer.

The implementation of the design has been developed using system C in accordance with Xilinx SDK/EDK tool kits. When the boards are restarted, they must download the codes on the WARP nodes through a USB cable while running the WARP boards and the console messages are shown in the warp drive and RTP source terminals by means of the SSH PuTTY. The power control mechanism was developed on the transmitter side only and the receiver power is the default power and it is adjustable.

In this case WARP nodes were used to test and verify the algorithms and concepts. In this setup, every WARP node contains its own host PC and by following the protocol stack, obtaining data packets from the enthernet and transferring them into exmac headers through the WARP drive, the data is trasnferring by means of a step-by-step process based on the designed protocol suite from the network layer to the MAC layer. According to the antenna considerations, the power levels are being operated from 0 to 63 (in decimal values), usually the power is represented in dBm. According to the maxim radio board datasheet, the values provided in [5] were followed and for the system level programming the power values in dBm were converted from binary to decimal values.

4.4 Measurement Setup

4.4.1 Test Scenario

This measurement setup was conducted in the indoor lab environment at Ericsson research lab, Kista, as shown in figure 4.7. The proposed mechanisms were developed for the point-to-point communication of Exnodes, to control the power levels between any pair of WARP Nodes, using a warp drive and rtp terminals which shows the data packet transmission and reception of foxy messages. The RTP SRC is a set of commands and it serves to operate the transmission and reception packet transaction of the ExMAC headers. The measurement setup serves the data packets transmission and the recpetion between the top layers, which are from the network(transport) layer to the physical layer. According to the power control mechanisms, they worked based on Network and MAC layer considerations. The warp drive is another console terminal used to display the packet transmision and reception sequence numbers and other messages, which are coming from the ExMAC headers.

Figure 4.7: Point-to-Point Communication Measurement Setup

This experimental setup assits in determining the tested results on the WARP drive and the RTP Source terminals. In the RTP src terminals, a list of commands is used to operate the console messages, which are displayed in the Appendix.

In this scenario, no scripting languages are being used for the continuous run to the point of target packets transmission/reception. Consideration was given to power control parameters, which were displayed in the WARP drive console terminals and these included gain, TX data packet sequence numbers and receiving packets of receiver sequence numbers and also feedback ACK sequence numbers, which appear on the WARP drive console terminals. In this case it was not possible to capture data continuously because the warp drive consoles were flushing (updating) continuously for every twenty packet transmission and reception. In order to achieve this, a measurement setup code has been written RTP source terminals in order to log the continuous data on seperate files using array funtions.

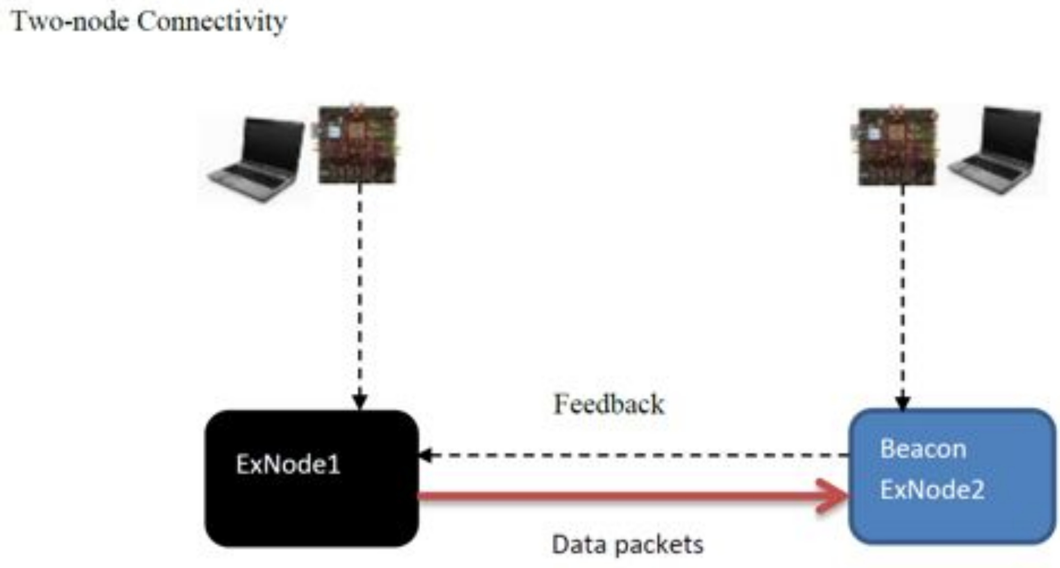

Figure 4.8: Two Node Measurement Setup

This measurement setup has been arranged with two nodes namely, Node1 and Beacon Node2 and another possible version involving three nodes as Node1, Node3 and Beacon Node2. In this case, the beacon node is a reference node and it delivers the connectivity between node1 and node3, which means whether it is synchronized (sync) or not (non-sync). It was always the case that the nodes were placed in order to be able to measure at different fixed distances and also to perform at different fixed time intervals through the RTP SRC. Each node had obtained its own unique color tag representation which specifies the difference between the nodes and every node has its own host PC.

The figure below represents the measurement setup of the controller PC with a pair of nodes. This controller has been monitored to test or verify the board's conditions as well as giving suggestions or considerations to the boards, as to whether they are working under normal conditions or not. By means of the controller with the USB, it is possible to always download the codes on WARP boards, while it is being used different applications, the evaluation of results and measurement setups have been conducted using this PC controller. These developed transmit power con-

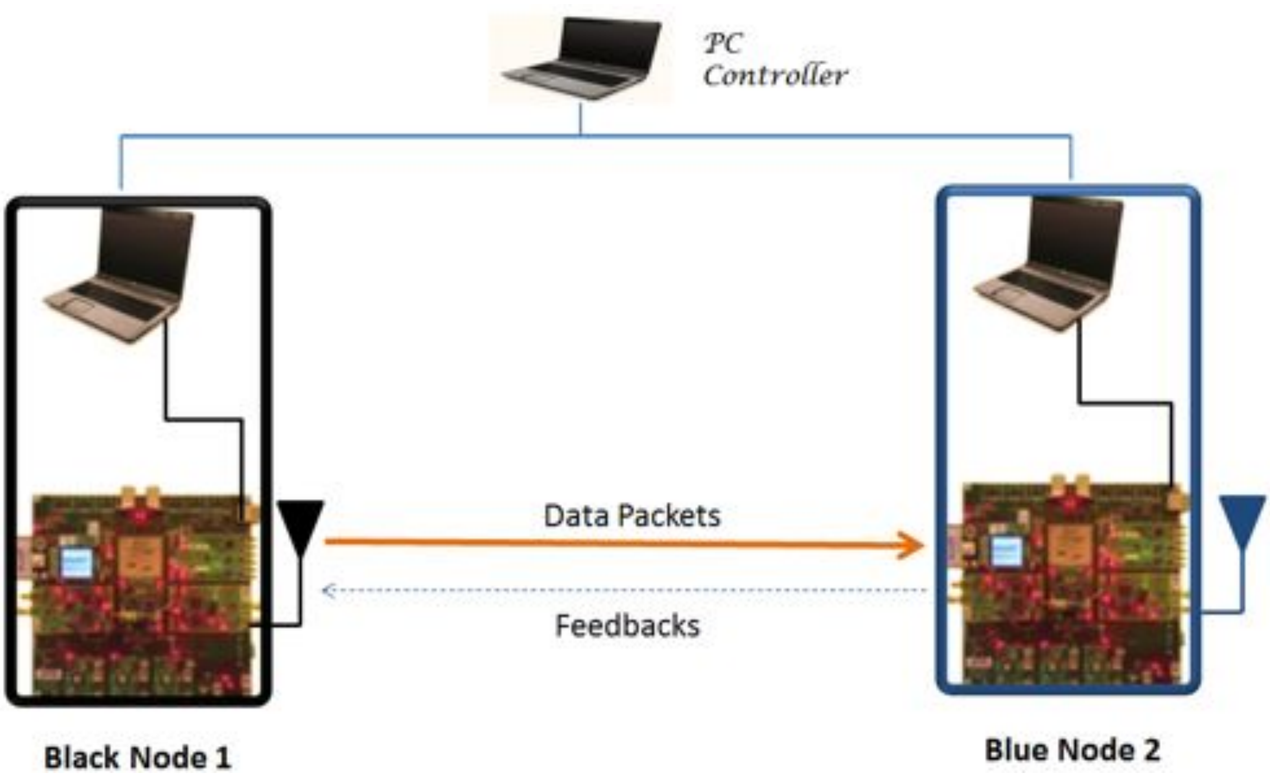

Figure 4.9: Point-to-Point Communication Measurement Setup

trol mechanisms are suitable for many communication system applications such as Device-to-Device, Network assisted device-to-device and adhoc networks, VANETs (Vehicular adhoc networks), MANETs (Mobile adhoc networks) and by enhancing these algorithms it may useful for many short range communication systems.

RESULTS AND DISCUSSIONS

5.1 Measurements

The measurement setup results are for the first and second transmitter power control mechanisms on WARP nodes, which represent different options in relation to of measurements for node-to-node communication. In this approach, several environmental challenges such as interference, losses and node efficiecy were considered and several measurement tests have been conducted through the PC controller. It also did not prove to be possible to measure the SINR as there was only a one way data tranmission setup such as node-to-node communication. In this scenario, the plots were made in order to observe the transmit power control at the sending node for the continuous packet transmission and also to account for the packet losses at receiving node.

This section provides the results for the transmit power control mechanism on WARP nodes. The measurment setup has been considered for the point-to-point communication at different fixed distances and different fixed time intervals. It is not always possible to move the nodes, and thus check the boards have to placed certain fixed distances in relation to measuring and, for this, the operating frequency of WARP node is 5GHz. The given results are plotted as transmit power versus (Vs.) number of transmitted packets.

5.1.1 Measurements Analysis

This section provides an analysis of the results, which contained measurement metrics, power control operating regions and tunable parameters. which regards to the transmitter power control, some tunable parameters have been considered so as to monitor the behavior of the nodes, regarding whether or not there is data transmission flow within the steady-state region under any circumstances. If the nodes were being faced with high or low interferences, then it is possible to tune the parameters for higher performances for continuous transmission over-the-air. These tunable parameters have been described with different possible performances for the power control mechanisms. Based on these considerations, it is possible to save the power as well as the packet loss rate and it thus become possible to define these considerations which were the best performers. In this scenario, different tunable parameters such as different window sizes, drop rates and drop steps were considered, based on these parameters, an analysis and tests have been conducted under different conditions. Thus if different window sizes are being considered this means that fixed drop rates and drop steps (power increase/decrease step level) and are being considered. According to the measurement analysis, two conditions for testing has been used namely power level up or power level down, and this involved different operating regions and tunable parameters.

1. In this section, transmit power control has been considered in order to check the operating regions such as the transient or steady-state regions. Transient region assist in showing the way to the steady-state region and based on this it is possible to calculate the power consumption, how much power is consumed to reach the steady-state region as well as how many packet errors would have been occured during the intial stage (transient) to steady-state. It is also possible to address the speed of convergence to the steady state region while under power ramping-up or down conditions.

2. Packet window size function was considered in an array, expressed in different sizes, which are shown in the table 5.1. This dealt with the transmit power control mechanism used to send the TX data packets through the packet window function to the reciver node. If the transmitter node receives the feedback ACKs of every successfully transmitted packets, then the window function considered these to be zeros ('0'). If the transmitted packets did not receive a feedback ACKs from the receiver, then the window fuction prints those packet losses (continuous transmitted packet sequence numbers) in the array. The main goal of this parameter consideration is in relation to controlling the packet loss rates. The window size was considered in different ranges from 2 to 10 and the measurements analysis for the tunable parameters were used. This packet window size will be varied according to the demands of the higher performances and this function works together with the packet drop rates and the power step sizes considerations, which means that if the packet window sizes are varied, then the packet drop rates and power step sizes are fixed. In this case, if the window size is to be tuned, then it increases the power consumption.

3. Packet Drop rates fixes the target range of the power level reduction and the current operating power step size provides sufficient or less than sufficient power and based on this, it will reduce or increase the power step sizes. This property has been involved together with packet window sizes and power step sizes. In this case, the drop rates will be varied and the window size and power step sizes are fixed. This property has been involved to tune the mechanism performances, in relation to the speed of convergence regarding the maintenance of the power step sizes within steady state threshold region. Based on this function, it is possible to tune the power levels as much as required under any circumstances. This packet drop rates has been considered to vary from 5 to 100 in packets.

4. This power step size property defines how to tune the power levels based on system demands. The property ranges considered were from 1 to 10 in terms of power step levels. In this case, the power step sizes will be varied and thus the packet window sizes and packet drop rates are fixed. This parameter is mainly

considered in relation to maintaining the better node connectivity under any environmental circumstances.

Transmit Power Control Measurements Considerations			
Measurement Metrics	Average TX Power and Packet Loss Rate(%)		
Power Control Operating Zones	Transient (Power Up/Down) and Steady State Regions		
Tunable Parameters			
a) Window Sizes	Variable Window Sizes [2, 3, 5, 7, 10]	Fixed Drop Rate	Fixed Power Step Size
a) Drop Rates	Variable Drop Rates [5, 10, 25, 35, 50, 75, 100]	Fixed Window size	Fixed Power Step Size
a) Power Step Sizes	Variable Power Step Sizes [1, 3, 5, 7, 10]	Fixed Window size	Fixed Drop Rate

Table 5.1: Table of Transmit Power Control Measurements Considerations

5.1.2 Transmitter Power control management system

This section focuses on a description of an evaluation of the results. The following graphs were considered to test and analyze under two conditions such as power up and power down, in order to be able to determine the power threshold value by averaging the power for tested conditions. It then becomes possible to know the threshold value from which to start the power value from the steady state region. This will also provide information concerning the threshold region and it will also be possible to reduce the power consumption and packet loss rate. The complete graphical representation has been analyzed and tested based on the above metrics. The following plots were based on the list of tabulations of metrics performace analysis for different tunable parameters in different regions. In this scenario, the graphs plotted are average power Vs. packet loss rate for different tunable parameters. In this case, there has been a separation and there are plots for the single metric (vs.) tunable parameters to provide an analysis of better performance metrics. The graphs below show the performance differences between different tunable parameters with the metrics and it is also possible to observe the performance of the tunable parameters under different measurement metrics. In this measurement analysis, we have done several test runs have been conducted in order to provide reliability for the performances of the tunable parameters, 10000 continuous packet transmissions have been conducted and if graphs for different window sizes are plotted then fixed drop rates and drop steps must also be considered. During the analysis, graphs were plotted when one parameter is to be varied while the other two are fixed. The measurement analysis has been based on the following formulas 5.1 and 5.2

$$\text{Average Power(AVGP)} = \frac{\text{Sum of individual packet TX power}}{\text{Total transmitted packets}} \tag{5.1}$$

$$\text{Packet Loss Rate (PLR)} = 1 - \frac{\text{Number of packets received}}{\text{Total packets transmitted}} * 100 \tag{5.2}$$

5.1.2.1 Transient Region

In this graph 5.1 describes the power ramp up transient region for different tunable parameters in relation to the metrics analysis and was used to measure how rapidly it converged to the steady state region and also to calculate the average power of the tunable parameters such as different packet window sizes, packet drop rates and power level drop and rise steps. The graphs shows the differences between changeable parameters, namely how much average power was consumed to reach the steady state threshold region from the lowest level (transient region) and which parameter is better than which. In this analysis, it is easier to determine the best rather than the poorest changeble parameters. The paremeters settings can then be easily tuned for the power levels under any circumstances.

The second graph 5.2 expresses the packet loss rate Vs. different tunable parameters. In this graph, the packet loss rate performances at different tunable parameters can be observed and also how it will vary, when the parameters considerations are changed. If the focus was on a higher quality of the signals or data packet transmission, then little more power than the original power value is consumed. In this scenario, packet loss rate is always inversly proportional to the average power.

This power ramp up transient region metrics analysis assisted in determining the steady state threshold region as well as the amount of time, how rapidly it converged and also able to address how many packet errors would occur during the packet transmission. The system efficiency can be determined and a closer look at the plots shows that there is little difference in the packet error rates while the packet transmission is from the lowest power level (transient region) to the steady state region. The average packet error rate is 0.23 percent at different window sizes and for different drop rates and the average power also has the same values for the different tunable parameters. In this scenario, the main differences were for different power step sizes of the transient region, meaning the power ramp up and down levels, it will vary based on parameter value of the drop step. As the drop step size increases, then more power will be consumed when compare with the others. This graph 5.3 explains the power

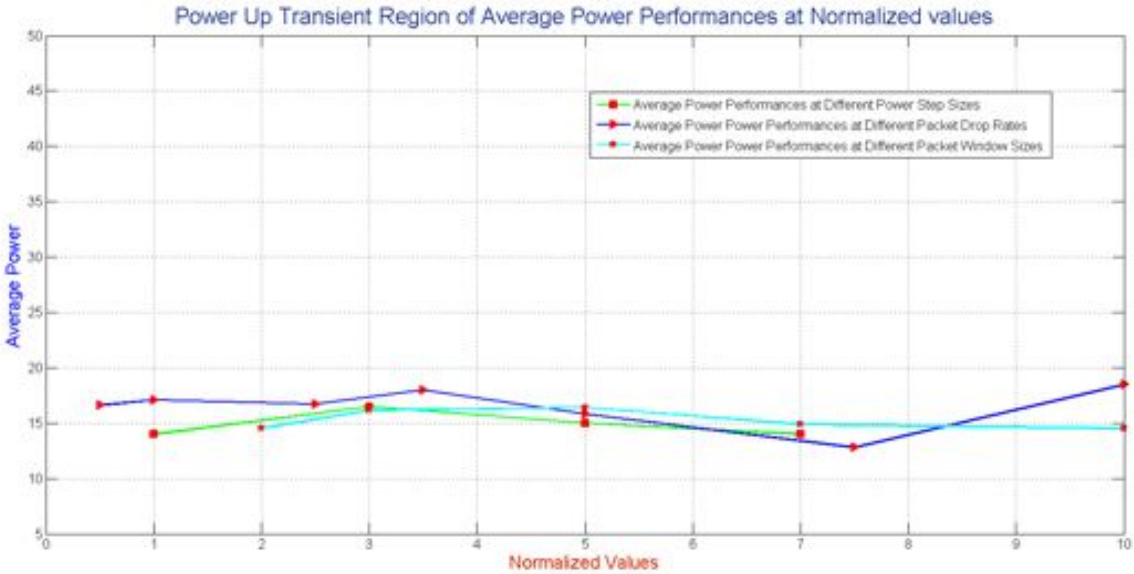

Figure 5.1: Power up Transient Region of Average Power Performaces at Different Tunable Parameters

ramp down case for the transient region, this test case is used to show the highest level of the power to the steady state threshold region. This test case has been analyzed under the worst circumstances for real environmental conditions. These can never be known accurately and they were thus tested and verified for the highest power level. In

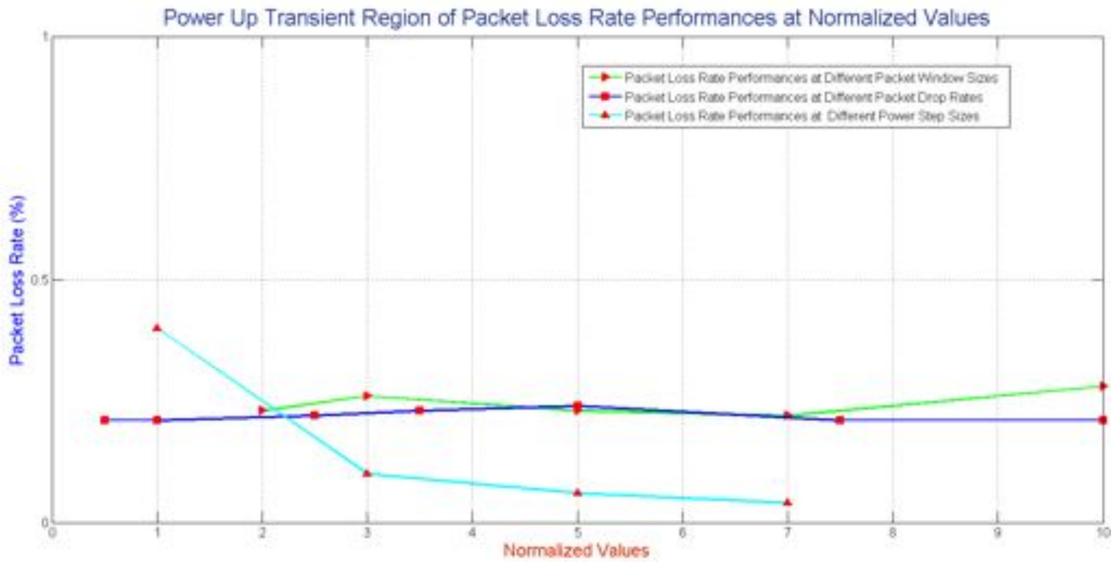

Figure 5.2: Power Up Transient Region of Packet Loss Rate Performaces at Different Tunable Parameters

addition, the interference power threshold will vary continuously and thus for, some of the unconditional situations power control mechanisms, they have been operated at the highest power levels, after which the normal stage (steady-state region) will occur and for this the average power at different tunable parameters has been calculated, including the speed of convergence to the steady state threshold, which parameters are faster and which tunable parameters save more energy. In this scenario, all the tunable parameters had the same performances for the different operations. A comparision of the three different drop rates showed that they consumed a lower power levels than others because, while varying the drop rate parameters, more time was taken to reach the steady state region. If consideration is given to reducing the power consumption, then consideration must be given to the fact that there is a reduced number of drop rates.

5.1.2.2 Steady-State Region

This section describes the steady state region of tunable parameters and their operations with regards to how they were performing for different parameters of the metrics. In graphs 5.4 and 5.5 the performance metrics at the steady state region show which metric (average power or packet loss rate) was working effectively for different tunable parameters such as different packet window sizes and different drop rates and drop steps. In this analysis, the reliable tunable parameters for reducing the packet loss rates as well as saving the energy (power) are known.

Regarding the figures for the steady state region performance analysis, there are

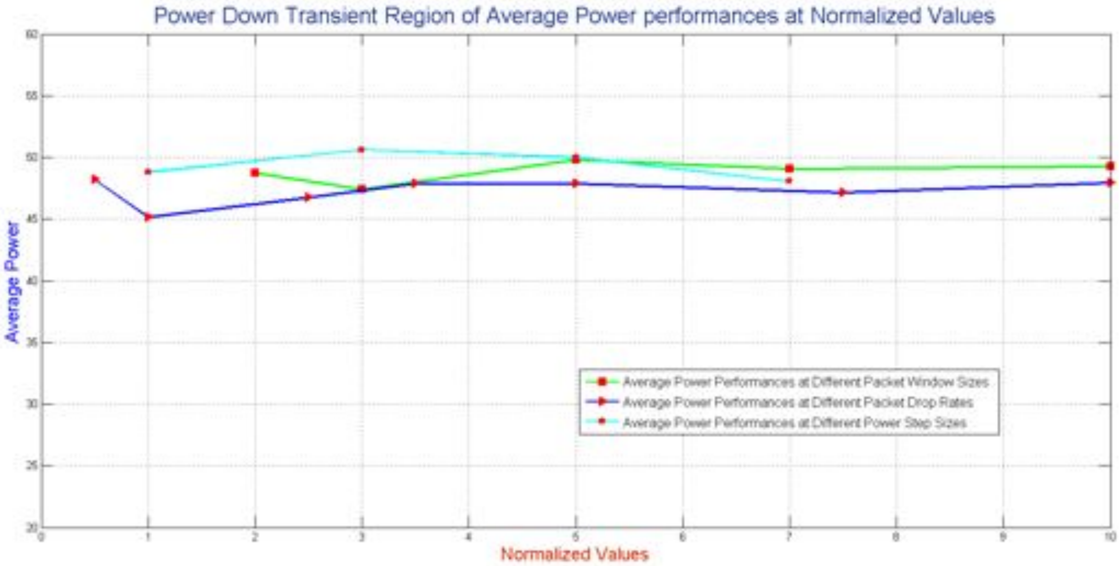

Figure 5.3: Power Down Transient Region of Average Power Performaces at Different Tunable Parameters

only minor differences between the lower and higher number of packet error rates and even the average packet error rate is less than 1% based on 10000 transmitted packets for different window sizes or drop rates or drop steps. The interesting aspect of the results is that the average power values are always within the steady state threshold region for different window sizes and drop rates. The different drop steps were consuming more power than was the case for the different window sizes and drop rates and there was almost equal packet error rates than was the case for the window sizes and drop rates. In this analysis, we can see that the different window size and drop rate parameters are performing better than the drop steps.

In this case, the transmit power control mechanism will always start from the steady state threshold region, thus power can be saved as well as some of the packet losses based on the above transient region suggestions. Particularly for the steady state regions, the average power is always inversly proportional to the packet loss rate. An increase in the power level to more than the threshold region that a 99.99 percent success rate is still not achieved and there is still a 0.02 percent packet error rate. In this scenario, the packet error rate can be reduced significantly as compared to the threshold region values, but it consumes more power than the threshold region, thus reducing the node efficiency. During this analysis, the power control mechanism has been shown to always have a significant impact on the transmission nodes, to control the node behavior under any circumstances and also to be able to control the nodes, performances to remain in the steady state threshold region, even if it is below or above the threshold region.

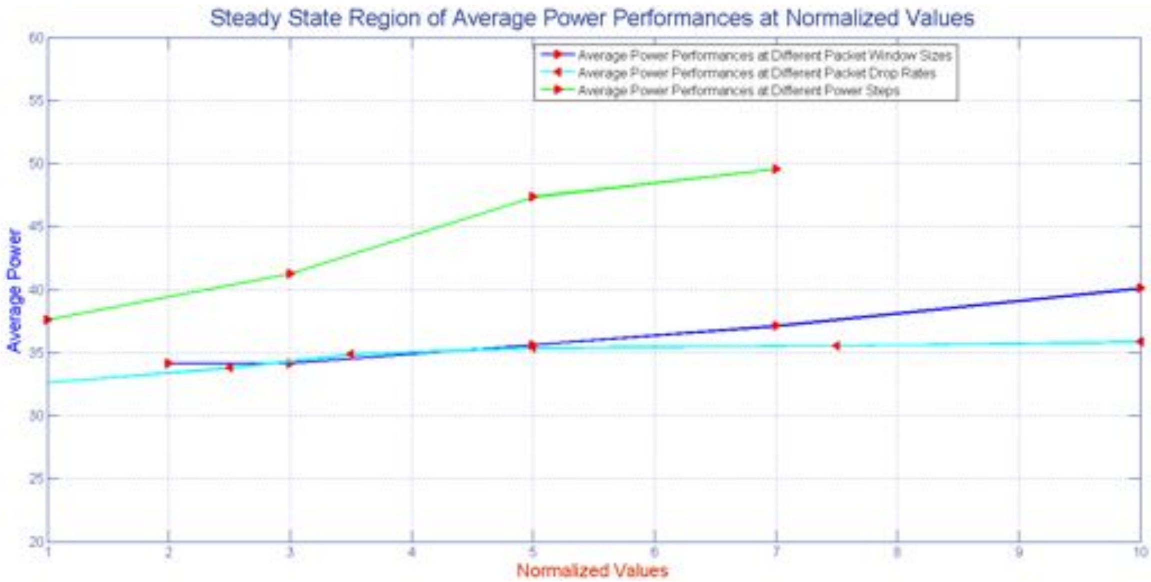

Figure 5.4: Steady State Region of Average Power Performaces at Different Tunable Parameters

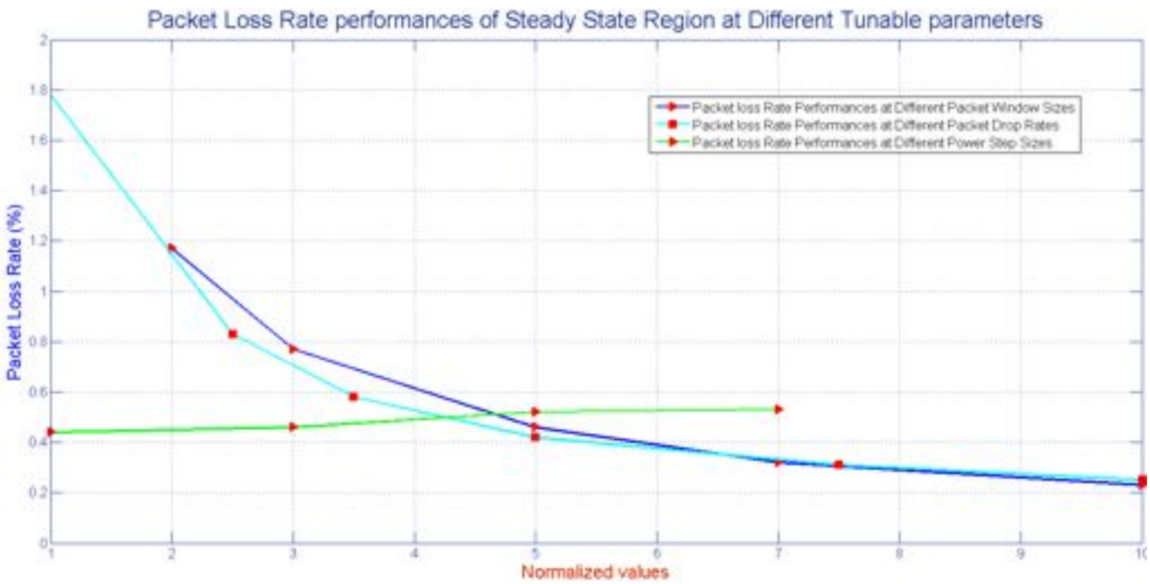

Figure 5.5: Steady State Region of Packet Loss Rate Performaces at Different Tunable Parameters

5.1.3 Without Window Function

This section mainly considered testing, how the transmit power control mechanism has performed without the window function and the followiing graphs have been measured in both the transient and steady-state regions. In this section the focus is on the system efficiency without the window function power control mechanism. In this scenario, the same tunable parameters have been considered with the exception of the window function considerations, which were used for the with window transmit power control mechanism.

5.1.3.1 Transient Region

Graphs 5.6, 5.7 and 5.8 show how much power was consumed and the packet losses which occured while conducting the power ramp up and ramp down (transient) conditions to reach the steady state threshold region. The graphs plots are based on the different packet drop rates and different power step sizes. In this case, the different power step sizes showed a greater impact than the different drop rates. Different drop rates were not capable in order to reduce the packet losses than was the case for the different power step sizes and power step sizes consumed slightly more power than was the case for the drop rates considerations.

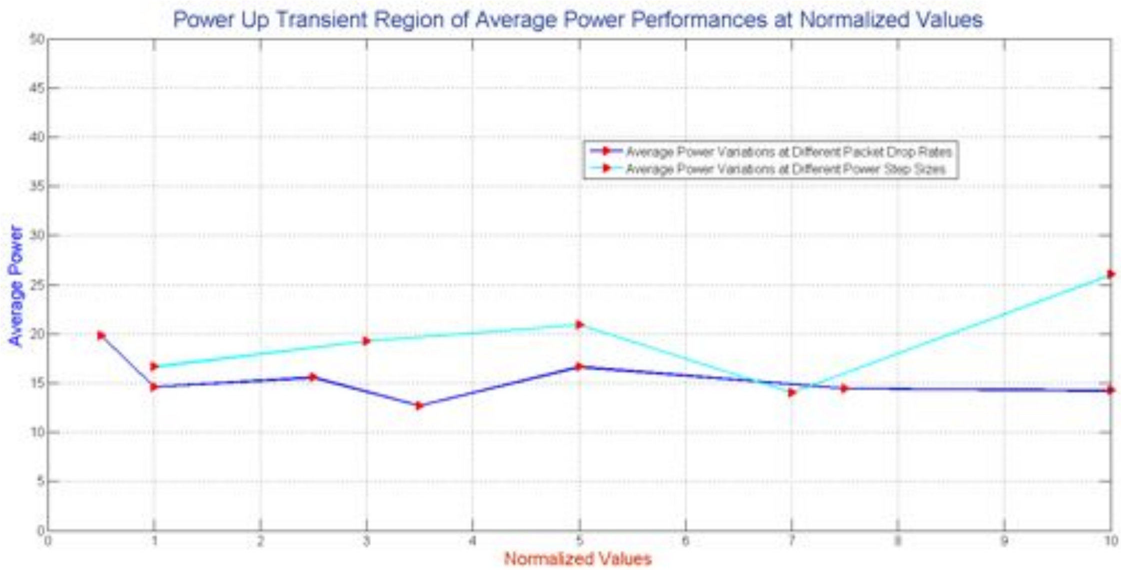

Figure 5.6: Power Up Transient Region of Average Power Performances at Different Tunable Parameters

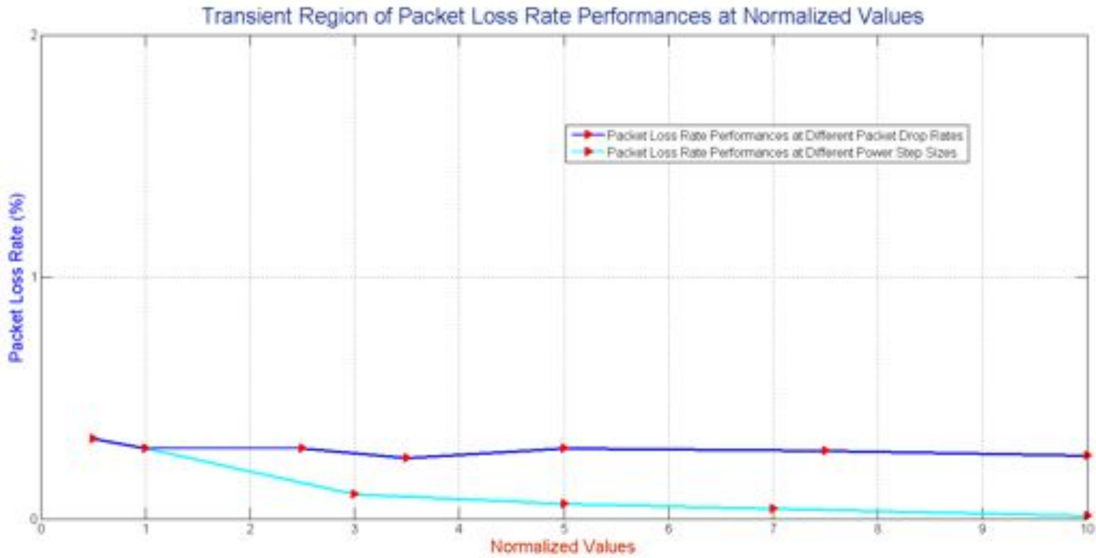

Figure 5.7: Power up Transient Region of Packet Loss Rate Performances at Different Tunable Parameters

Figure 5.8: Powe Down Transient Region of Average Power Performances at Different Tunable Parameters

5.1.3.2 Steady State Region

In graphs 5.9 and 5.10 the steady state region for the average power and packet loss rate performances at different tunable parameters are shown. In these graphs, the measurement metric performances for different tunable parameters can be observed, the different power step size considerations were also shown to provide better performances than the different drop rates. If graph 5.10 is observed it can be seen that the packet loss rate for the different power step sizes are stabilized as compared to the different packet drop rates, causing the heavy packet loss rate differences for the different drop rate considerations.

In this investigation, an intersting aspect of the average power has been observed in relation to achieving, minimum operating power levels rather than the packet loss rate. This meachanism has shown a better performances than, for what with the window function of power control mechanism. If the two cases (with and without window functions) are compared then, the major disadvantage for the without window function was not that it converged too aggressively reliable than the with window funtion because of the reduced parameter considerations.

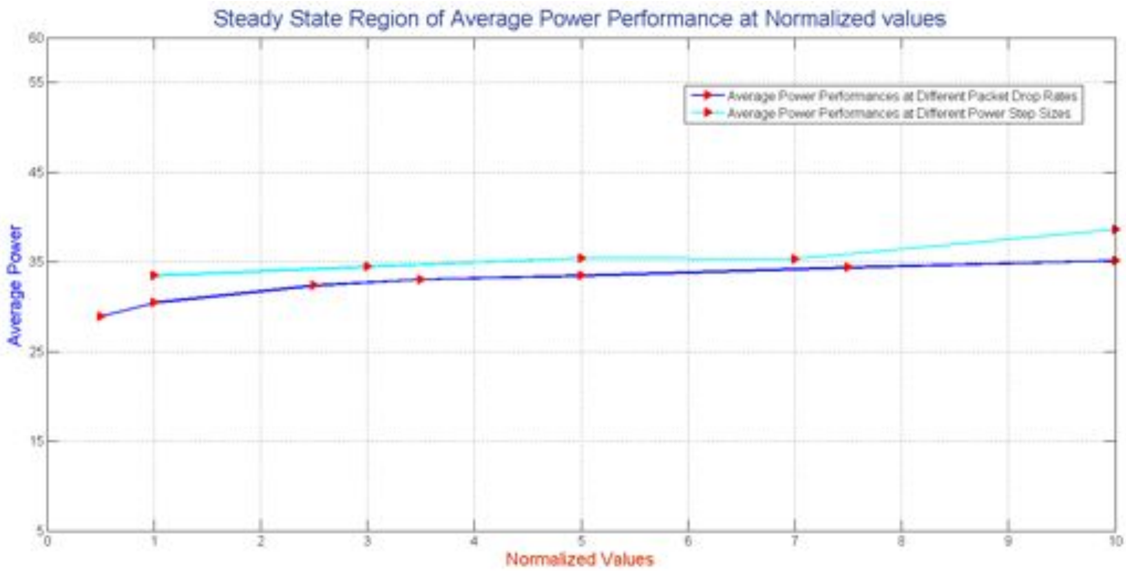

Figure 5.9: Steady State Region of Average Power Performances at Different Tunable Parameters

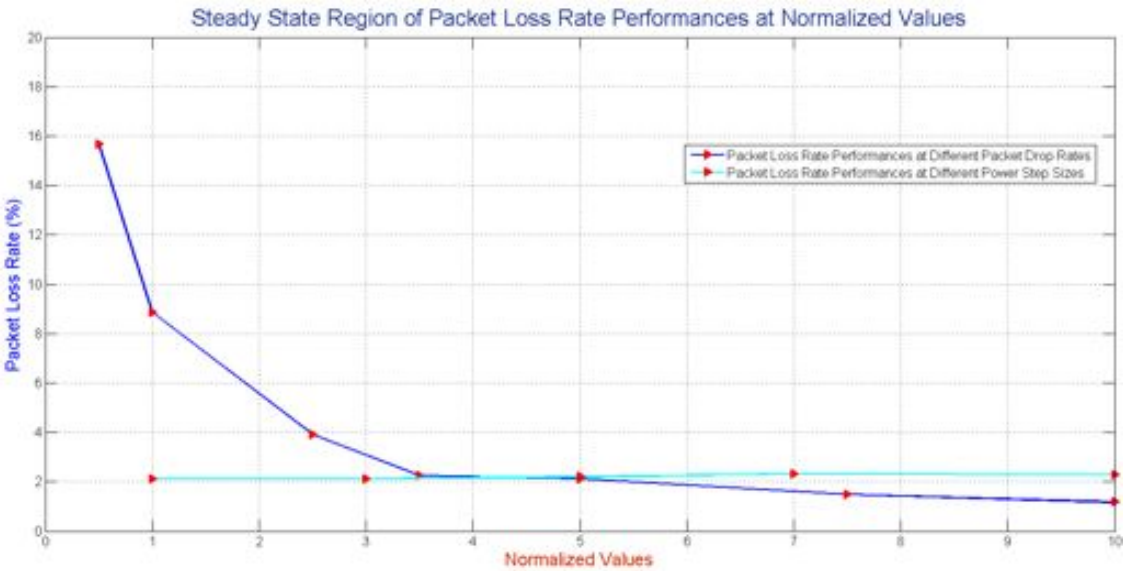

Figure 5.10: Steady State Region of Packet Loss Rate Performances for the Different Tunable Parameters

CONCLUSIONS AND FUTUREWORK

6.1 Conclusion

In this thesis, the main goal was to propose and develope new prototype transmit power control mechanisms on WARP boards for point-to-point communication, to reduce packet loss rate and power consumption. In the literature study, many power control mechanisms have been implemented in both simulation and practice for different communications. In this investigations it has been observed that many power control mechanisms have been implemented in simulation setups for multiple channel communications based on the mathematical proof of concepts. According to this approach and based on the limited scope of the work, a simple feedback ACK power control approach was proposed, which did not exist in either simulation or practice for point-to-point communications. This work has been implemented and tested in the real test-bed environments at Ericsson Research Laboratory, Kista, Stockholm in Sweden.

In this implementation, a new prototype had been designed and developed with and without window function power control mechanisms on WARP boards as described in chapter 3. Both the with and without window functions have involved measurement metric performances for different tunable parameters such as packet window sizes, drop rates and power step sizes.

From the results and dicsussions in chapter 4, the different metric performances for different tunable parameters can be seen and it was also possible to observe how the average power and packet loss rate performaces have varied during continuous transimission.

In this investigations, the tunable parameters for different window sizes and different drop rates have been observed to have the better performances than different power step sizes in both transient and steady-state regions. The window function property of the power control mechansim performed faster than the without window function property. In this scenario, the window function was shown to be more effective in relation ro packet loss rate performances than the without window funtion property. Moreover, the power control mechanism with the window function did not show less power consumption values than without window function power control mechanism.

The performances of the TPCM algorithm on WARP testbeds were based on a indoor environment. In this scenario, the experimental results showed that the without window function TPCM can save 10%-to-12% power consumption at different power step levels than was the case for the with window function TPCM. Additionally, the

TPCM with packet window function achieved a 99% packet reception rate betweeen the point-to-point communication than was the case for the without packet window TPCM algorithm.

The main advantage of the without window function was that it had better low power consumed values than was the case for the with window funtion property and that the without window was not sufficient to control a reduction in the packet error values than was the case for the with window function power control mechanism.

6.2 Future Work

This thesis has been focused so that there are expansions possible in many directions, First of all, consider to design and develop a further implementation of RSSI feedback concept together with ACK. This concept would involve an extension of the RSSI feedback transmit power control mechanism on WARP boards, which, because of time contraints, has not yet been implemented. An improvement in the RSSI feedback power control mechanisms including the addition of more features in order to provide higher system performances while consuming the less power levels is also of interest for this topic.

Secondly, another extension for this work is to measure the link quality indicator (LQI) of multiple pair of the nodes or MIMO communication systems. In this case, it should overcome the minor drawbacks of RSSI performances while performing with communication links. Another property involving a feedback ACK approach together with RSSI and LQI, would also be very interesting method in order to determine accurate system performances on WARP testbeds for future wireless networks.

Thirdly, it would be interesting to design and implement the mechanisms on WARP boards for advanced communication systems such as Single Input Multiple Outputs (SIMO), MIMO (Multiple-Input Multiple-Output), etc. In these cases, SINR parameters would be considered as new challenges may arise while considering these parameters. In this scenario, it is strongly recommended to design and develop the mechanisms on both the transmitter and receiver sides, because it is difficult to control the multiple channel parameters only on the tarnsmitter side.

Finally, the main extension to the work in relation to future wireless network systems would involve (D2D) Device-to-Device communication, Network-assisted D2D communications, etc.

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APPENDIX

A.1 Appendix A

A.1.1 WARP and RTP Commands

Commands name	Value	Description
Reset (r)	*	Reset the system
Flush (f)	*	Flush the system
Power (p)	0-63	Operating Power ranges in decimal
Code Rate (c)	0,1,2	Change the code rate among 1, 1/3 and 1/2
Interleaving (i)	0,1	Change interleaving

Table A.1: WARP Commands

Option	Value	Description
-d	hostname	Name or IP address of destination host (TX mode only)
-c	const idt	TX-mode constant inter departure times in ms (default = 40ms)
-n	Number of packets	Number of packets to TX in TX-mode; default = continuous
-t	talkspurts	Generate a talkspurt every 'talkspurts' no of packets
-s	IP frame size	Length of the TXd IP frame (in octets: 56-1500)
-f		Fill RTP payload with shifting "fox" message
-l	Listen duration	Duration receiving host listens for packets (in seconds)
-w	File name	Logs Rxd data into <filename> (default='/dev/null')
-a	File name	Like –w above, but append logs to <filename>')
-p	Port number	UDP port number (default = 8788)

Table A.2: RTP Commands

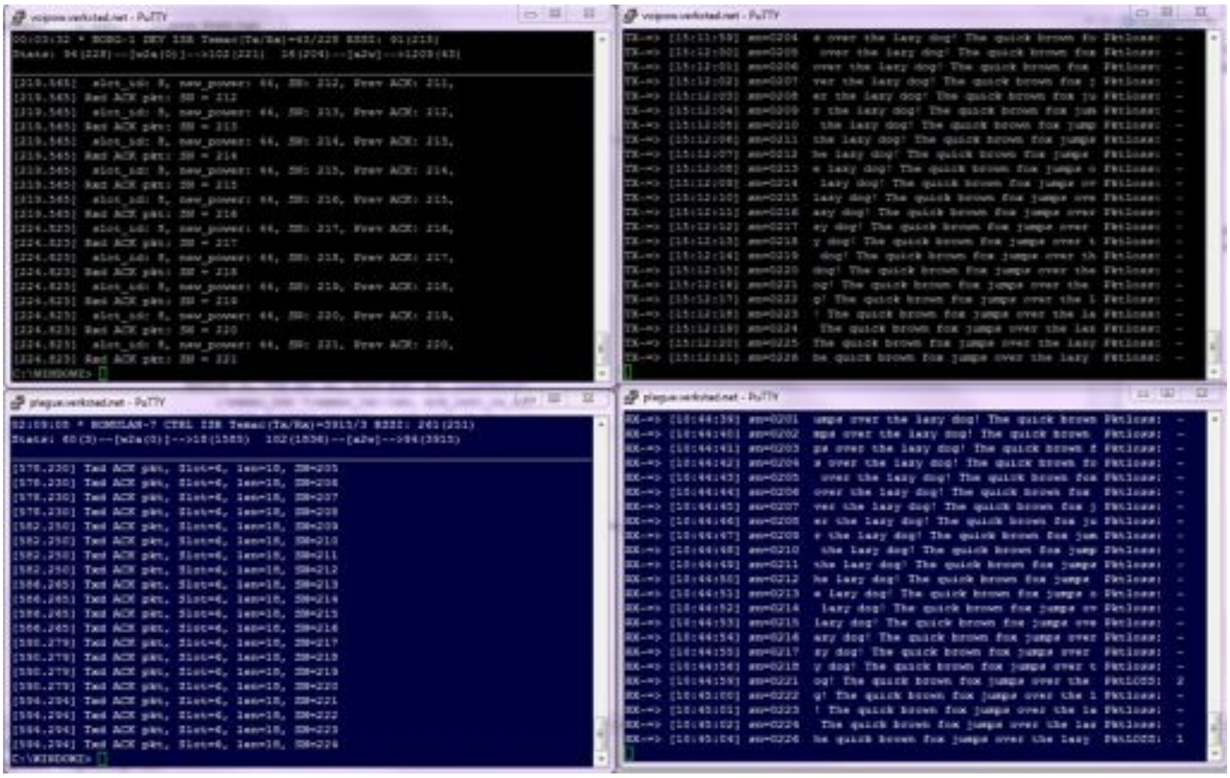

Table A.3: RTP Console Terminals

A.2 Appendix B

A.2.1 Additional Results of Transmit Power Control Mechanisms

Figure A.1: Transient Region of Different Window Sizes

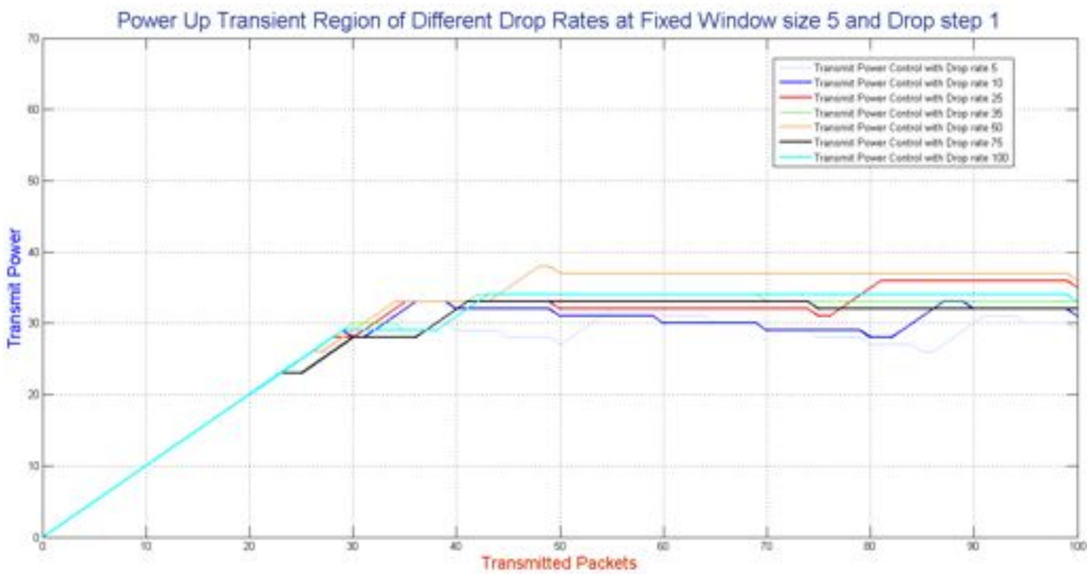

Figure A.2: Transient Region of Different Drop Rates

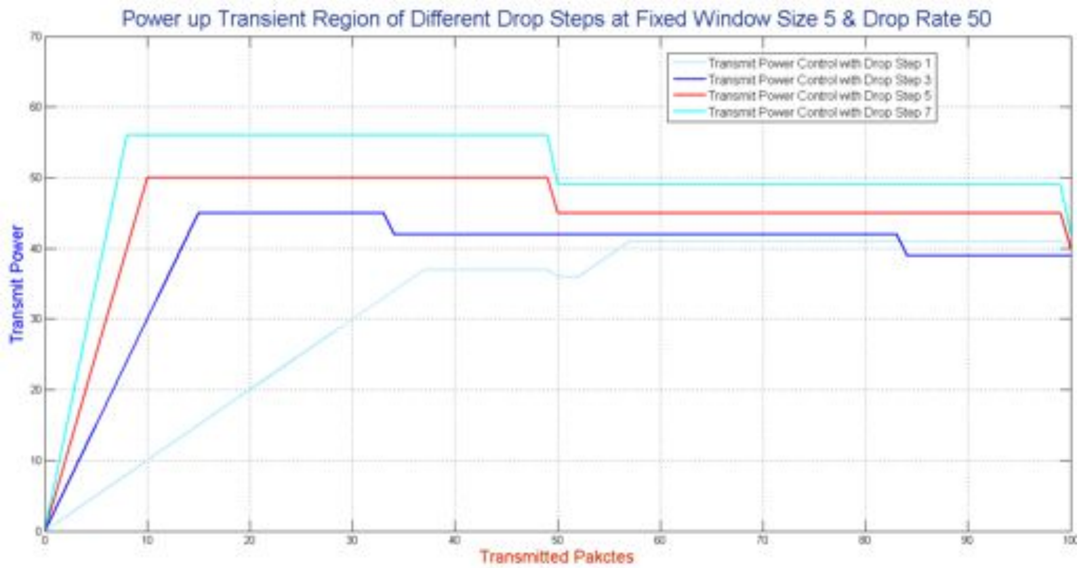

Figure A.3: Transient Region of Different Drop Steps

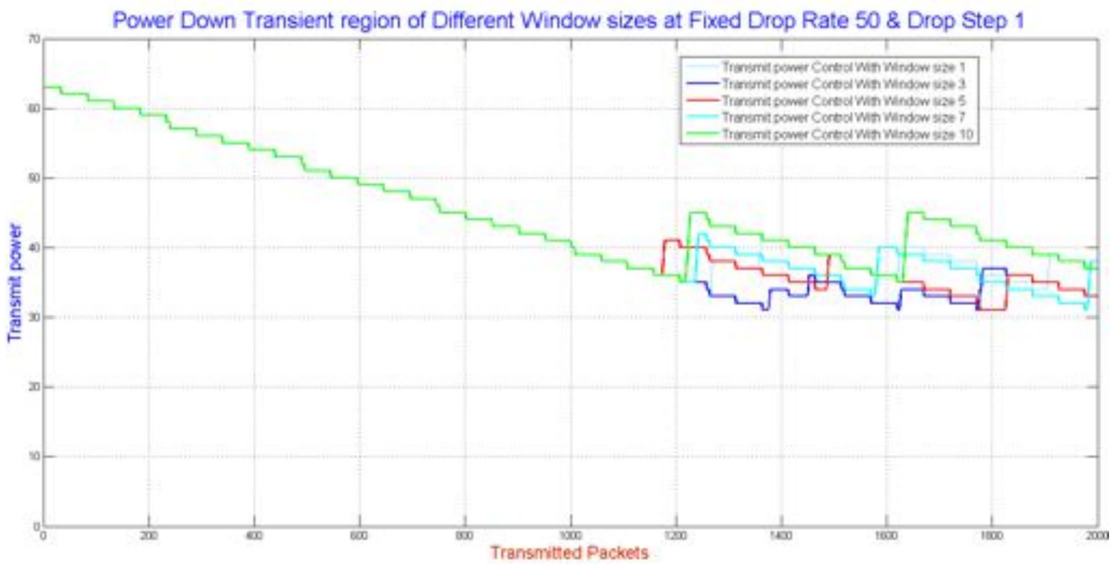

Figure A.4: Transient Region of Different Drop Rates

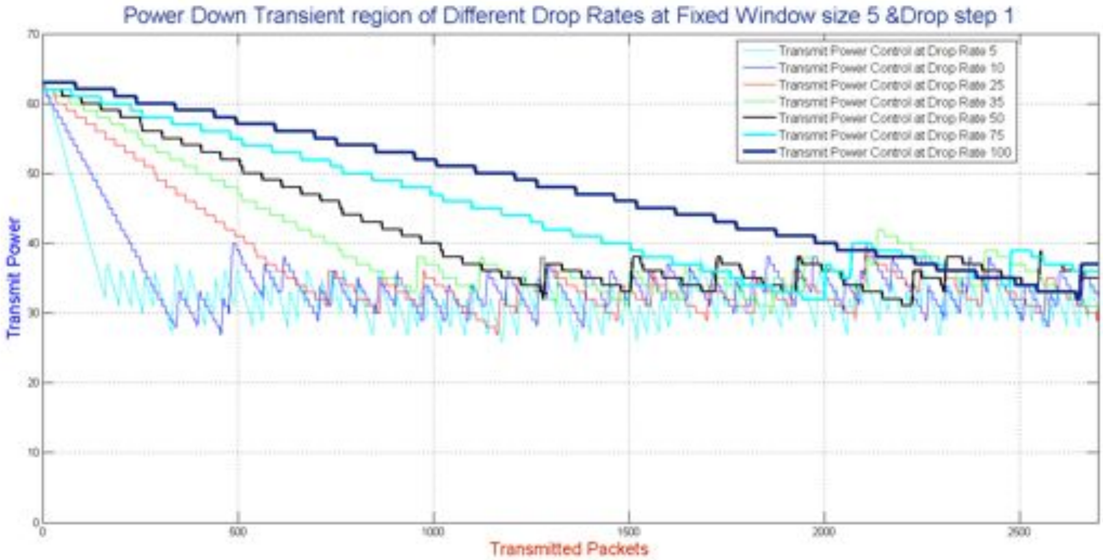

Figure A.5: Transient Region of Different Drop Rates

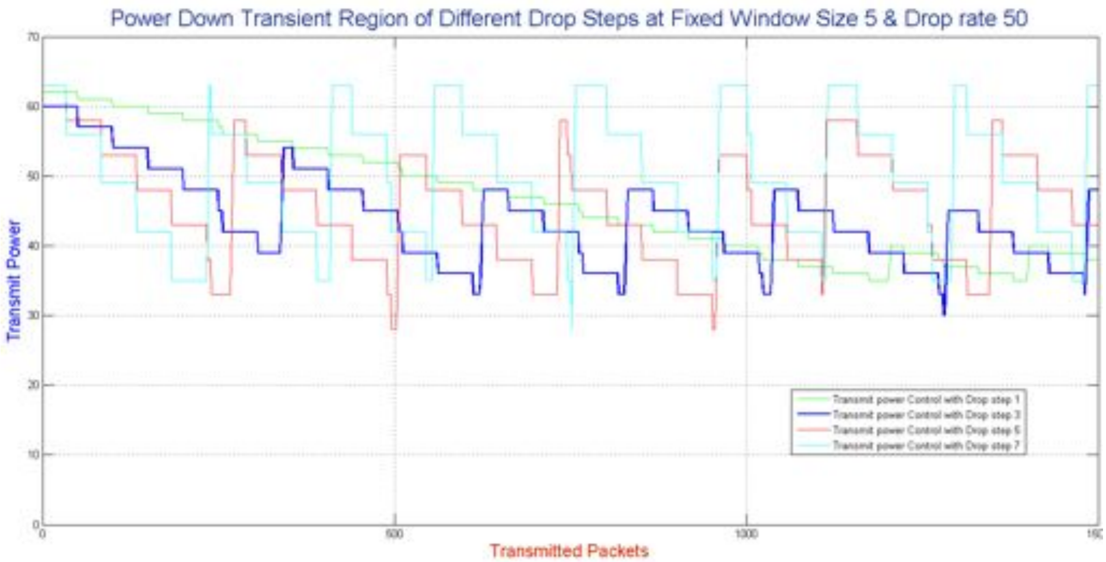

Figure A.6: Transient Region of Different Drop Rates

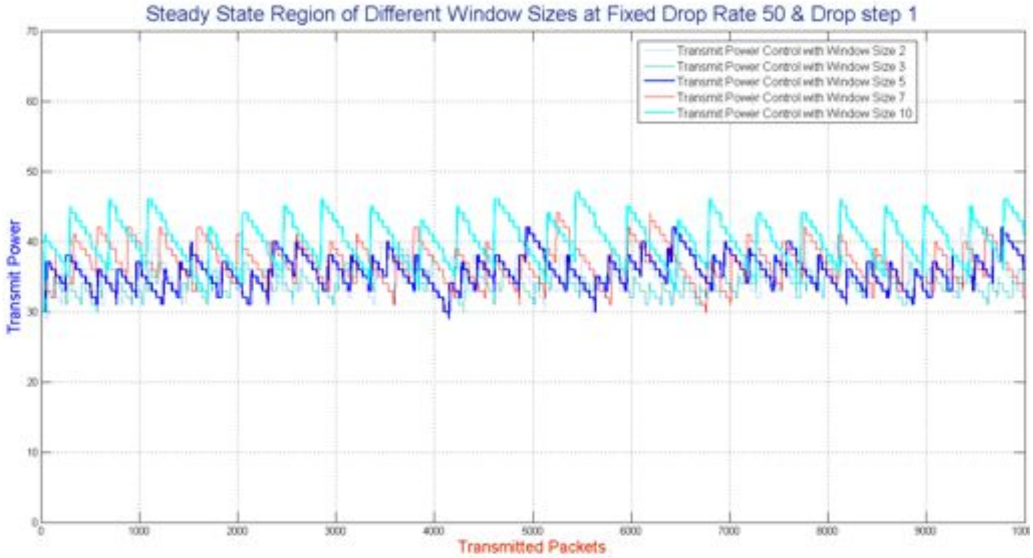

Figure A.7: Steady State Region of Different Window Sizes

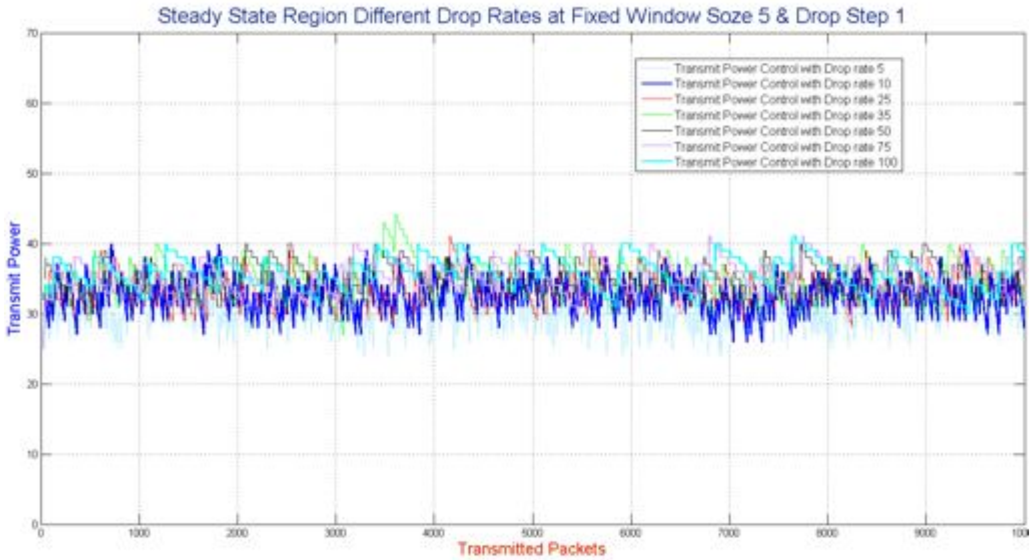

Figure A.8: Steady State Region of Different Drop Rates

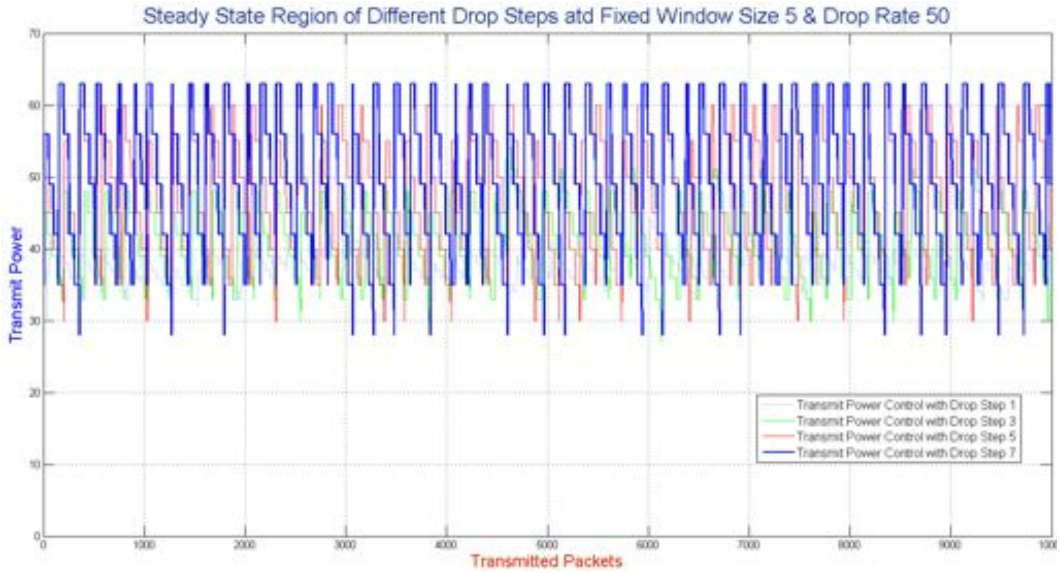

Figure A.9: Steady State Region of Different Drop Steps

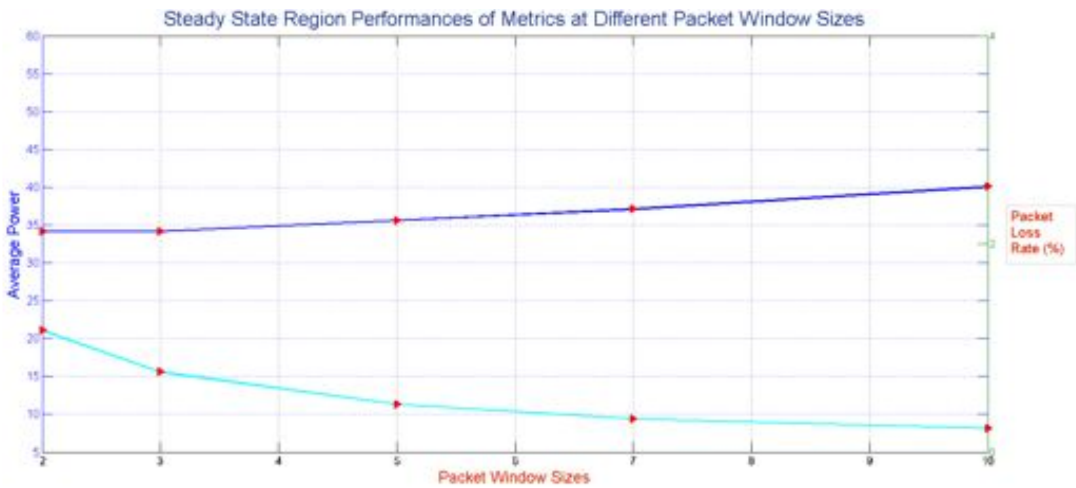

Figure A.10: Steady State Region of Different Window Sizes Performaces at Measurement Metrics

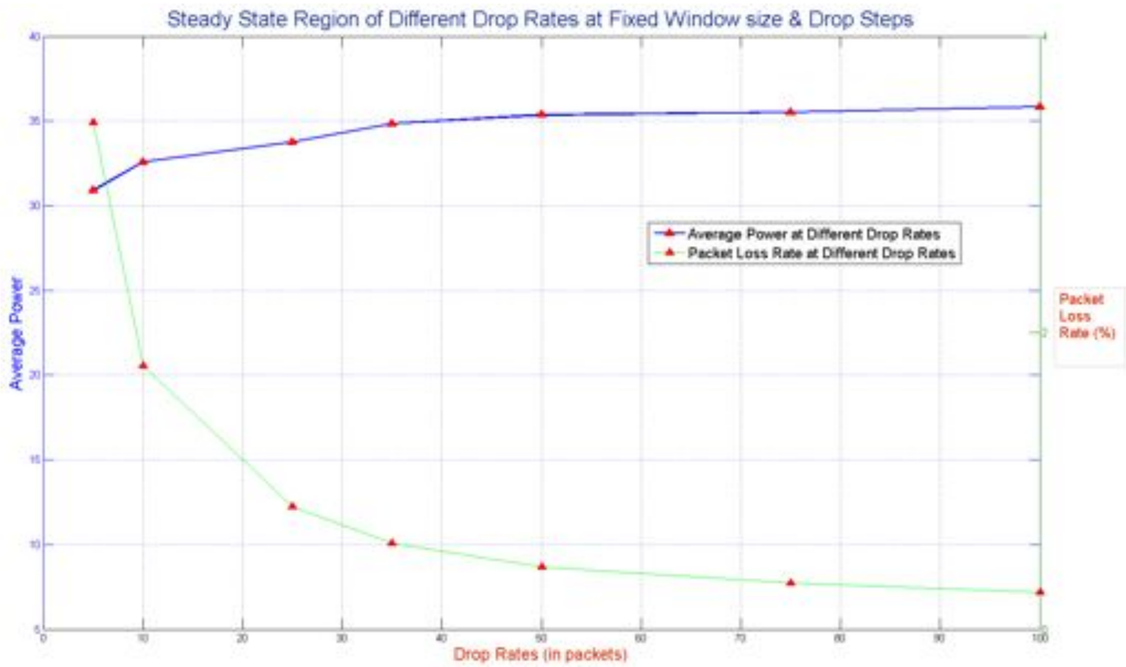

Figure A.11: Steady State Region Performace Metrics at Different Drop Rates

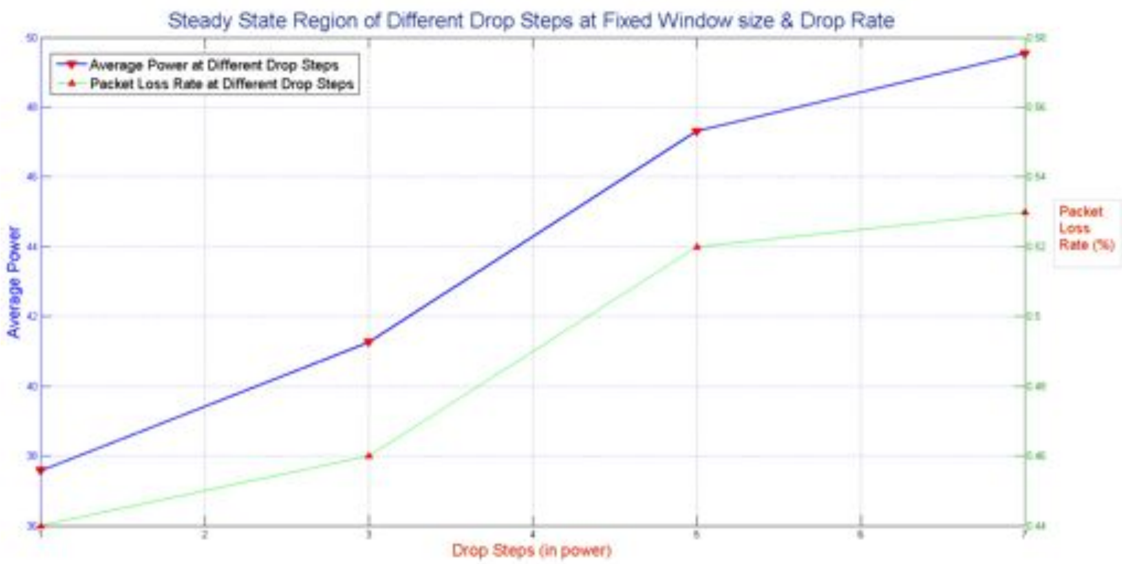

Figure A.12: Steady State Region of Different Drop Steps Performaces at Measurement Metrics