WARP FPGA Board

Rev 1.1 - December 2005

Patrick Murphy

Schematic Pages:

Rice University

Title
WARP FPGA Board

Description
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Rev
1.1

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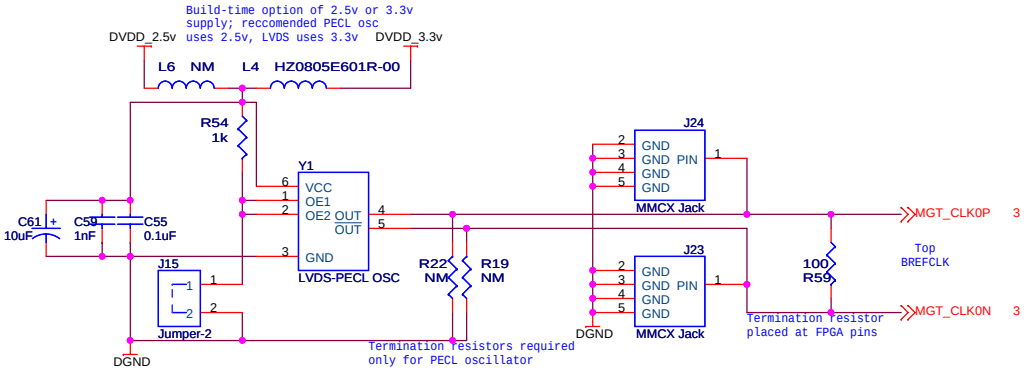

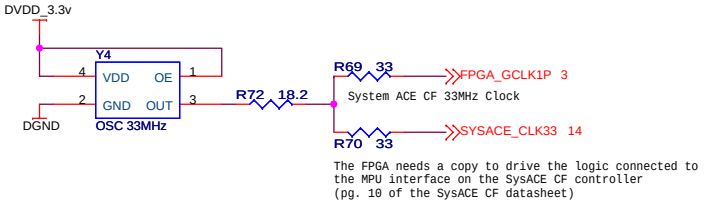

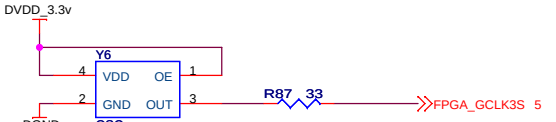

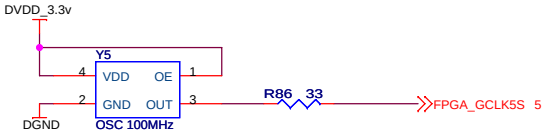

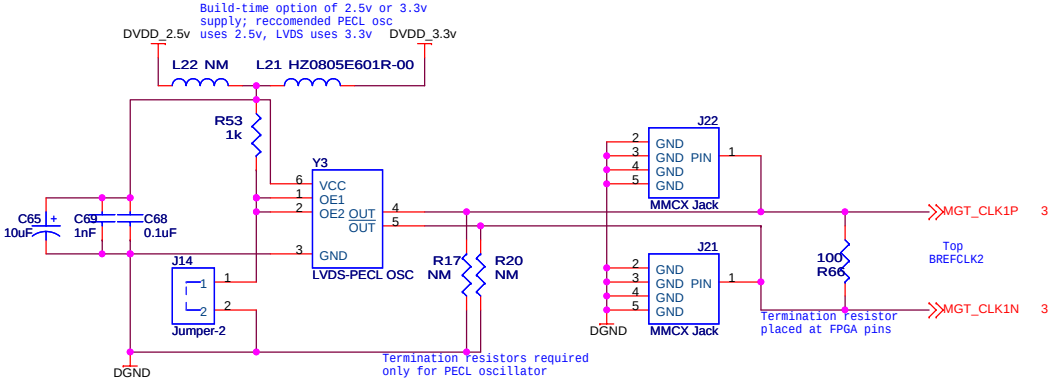

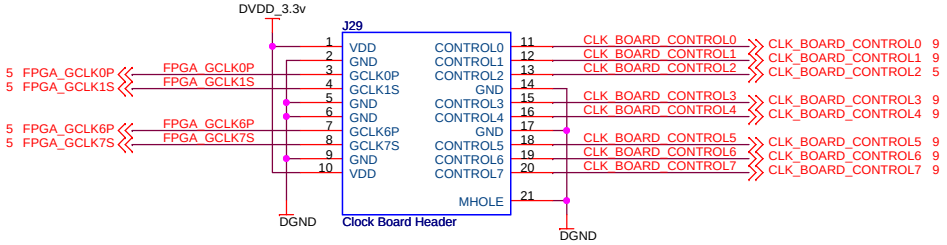

Rice University			
Title: WARP FPGA Board			
Description: Clocks			Rev: 1.1
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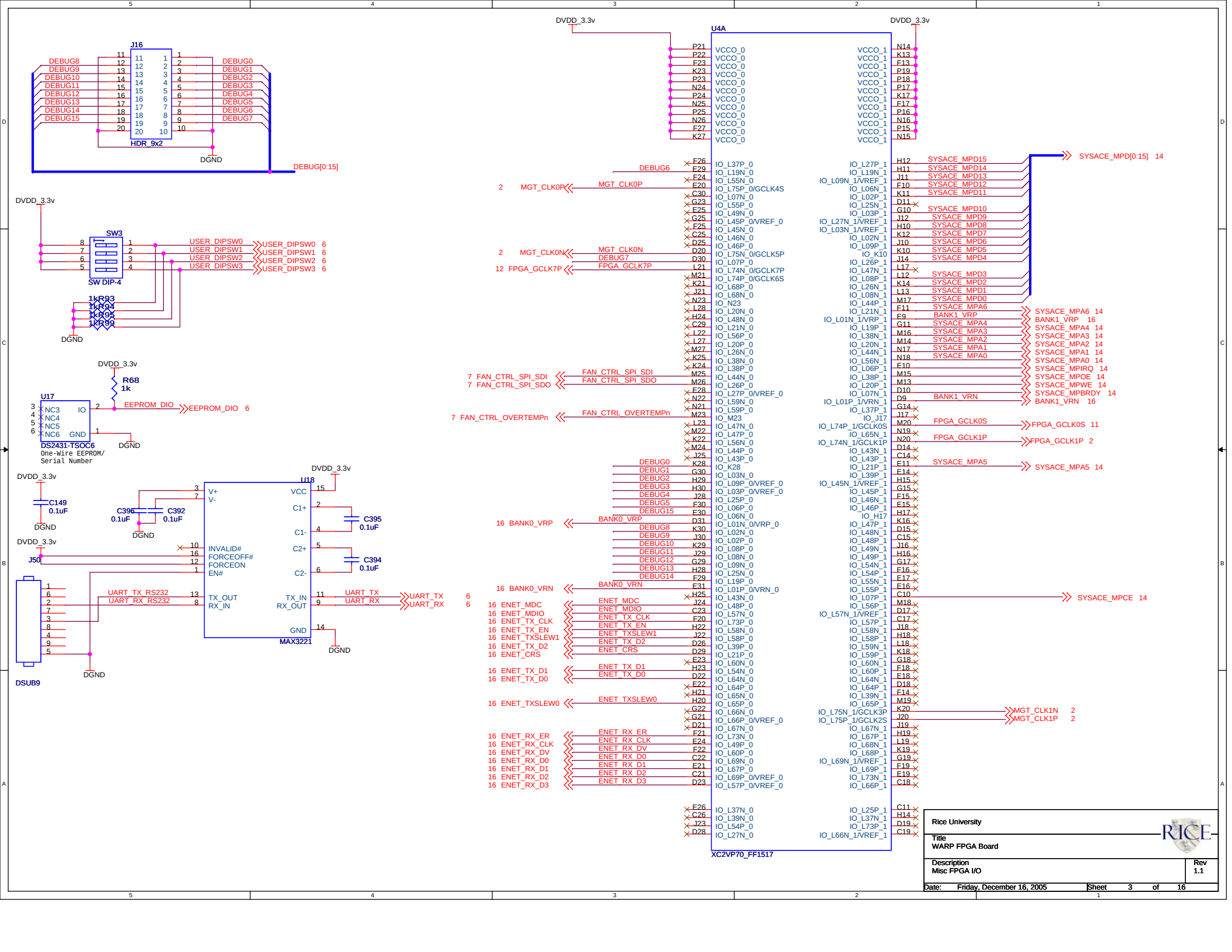
J16
HDR_9x2
DEBUG8
DEBUG9
DEBUG10
DEBUG11
DEBUG12
DEBUG13
DEBUG14
DEBUG15
DEBUG0
DEBUG1
DEBUG2
DEBUG3
DEBUG4
DEBUG5
DEBUG6
DEBUG7
DGND
DEBUG[0:15]
DVDD_3.3v
SW3
SW DIP-4
USER_DIPSW0
USER_DIPSW1
USER_DIPSW2
USER_DIPSW3
USER_DIPSW0 6
USER_DIPSW1 6
USER_DIPSW2 6
USER_DIPSW3 6
1kR93
1kR94
1kR95
1kR96
U17
DS2431-TSOC6
One-Wire EEPROM/
Serial Number
R68
1k
EEPROM_DIO
EEPROM_DIO 6
C149
0.1uF
C396
0.1uF
C392
0.1uF
U18
MAX3221
V+
V-
VCC
C1+
C1-
C2+
C2-
INVALID#
FORCEOFF#
FORCEON
EN#
TX_OUT
RX_IN
TX_IN
RX_OUT
GND
C395
0.1uF
C394
0.1uF
J50
DSUB9
UART_TX_RS232
UART_RX_RS232
UART_TX
UART_RX
UART_TX 6
UART_RX 6
U4A
XC2VP70_FF1517
VCCO_0
VCCO_1
IO_L37P_0
IO_L19N_0
IO_L55N_0
IO_L75P_0/GCLK4S
IO_L07N_0
IO_L55P_0
IO_L49N_0
IO_L45P_0/VREF_0
IO_L45N_0
IO_L46N_0
IO_L46P_0
IO_L75N_0/GCLK5P
IO_L07P_0
IO_L74N_0/GCLK7P
IO_L74P_0/GCLK6S
IO_L68P_0
IO_L68N_0
IO_N23
IO_L20N_0
IO_L48N_0
IO_L21N_0
IO_L56P_0
IO_L20P_0
IO_L26N_0
IO_L38N_0
IO_L38P_0
IO_L44N_0
IO_L26P_0
IO_L27P_0/VREF_0
IO_L59N_0
IO_L59P_0
IO_M23
IO_L47N_0
IO_L47P_0
IO_L56N_0
IO_L44P_0
IO_L43P_0
IO_K28
IO_L03N_0
IO_L09P_0/VREF_0
IO_L03P_0/VREF_0
IO_L25P_0
IO_L06P_0
IO_L06N_0
IO_L01N_0/VRP_0
IO_L02N_0
IO_L02P_0
IO_L08P_0
IO_L08N_0
IO_L09N_0
IO_L25N_0
IO_L19P_0
IO_L01P_0/VRN_0
IO_L43N_0
IO_L48P_0
IO_L57N_0
IO_L73P_0
IO_L58N_0
IO_L58P_0
IO_L39P_0
IO_L21P_0
IO_L60N_0
IO_L54N_0
IO_L64N_0
IO_L64P_0
IO_L65N_0
IO_L65P_0
IO_L66N_0
IO_L66P_0/VREF_0
IO_L67N_0
IO_L73N_0
IO_L49P_0
IO_L60P_0
IO_L69N_0
IO_L67P_0
IO_L69P_0/VREF_0
IO_L57P_0/VREF_0
IO_L37N_0
IO_L39N_0
IO_L54P_0
IO_L27N_0
IO_L27P_1
IO_L19N_1
IO_L09N_1/VREF_1
IO_L06N_1
IO_L02P_1
IO_L25N_1
IO_L03P_1
IO_L27N_1/VREF_1
IO_L03N_1/VREF_1
IO_L02N_1
IO_L09P_1
IO_K10
IO_L26P_1
IO_L47N_1
IO_L08P_1
IO_L26N_1
IO_L08N_1
IO_L44P_1
IO_L21N_1
IO_L01N_1/VRP_1
IO_L19P_1
IO_L38N_1
IO_L20N_1
IO_L44N_1
IO_L56N_1
IO_L06P_1
IO_L38P_1
IO_L20P_1
IO_L07N_1
IO_L01P_1/VRN_1
IO_L37P_1
IO_J17
IO_L74P_1/GCLK0S
IO_L65N_1
IO_L74N_1/GCLK1P
IO_L43N_1
IO_L43P_1
IO_L21P_1
IO_L39P_1
IO_L45N_1/VREF_1
IO_L45P_1
IO_L46N_1
IO_L46P_1
IO_H17
IO_L47P_1
IO_L48N_1
IO_L48P_1
IO_L49N_1
IO_L49P_1
IO_L54N_1
IO_L54P_1
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IO_L64P_1
IO_L39N_1
IO_L65P_1
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IO_L75P_1/GCLK2S
IO_L67N_1
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IO_L68N_1
IO_L68P_1
IO_L69N_1/VREF_1
IO_L69P_1
IO_L73N_1
IO_L66P_1
IO_L25P_1
IO_L37N_1
IO_L73P_1
IO_L66N_1/VREF_1
SYSACE_MPD15
SYSACE_MPD14
SYSACE_MPD13
SYSACE_MPD12
SYSACE_MPD11
SYSACE_MPD10
SYSACE_MPD9
SYSACE_MPD8
SYSACE_MPD7
SYSACE_MPD6
SYSACE_MPD5
SYSACE_MPD4
SYSACE_MPD3
SYSACE_MPD2
SYSACE_MPD1
SYSACE_MPD0
SYSACE_MPA6
BANK1_VRP
SYSACE_MPA4
SYSACE_MPA3
SYSACE_MPA2
SYSACE_MPA1
SYSACE_MPA0
SYSACE_MPIRQ
SYSACE_MPOE
SYSACE_MPWE
SYSACE_MPBRDY
BANK1_VRN
SYSACE_MPA5
FPGA_GCLK0S
FPGA_GCLK1P
SYSACE_MPCE
MGT_CLK1N
MGT_CLK1P
SYSACE_MPD[0:15] 14
SYSACE_MPA6 14
BANK1_VRP 16
SYSACE_MPA4 14
SYSACE_MPA3 14
SYSACE_MPA2 14
SYSACE_MPA1 14
SYSACE_MPA0 14
SYSACE_MPIRQ 14
SYSACE_MPOE 14
SYSACE_MPWE 14
SYSACE_MPBRDY 14
BANK1_VRN 16
FPGA_GCLK0S 11
FPGA_GCLK1P 2
SYSACE_MPA5 14
SYSACE_MPCE 14
MGT_CLK1N 2
MGT_CLK1P 2
2 MGT_CLK0P
MGT_CLK0P
2 MGT_CLK0N
MGT_CLK0N
12 FPGA_GCLK7P
FPGA_GCLK7P
DEBUG6
DEBUG7
7 FAN_CTRL_SPI_SDI
7 FAN_CTRL_SPI_SDO
FAN_CTRL_SPI_SDI
FAN_CTRL_SPI_SDO
7 FAN_CTRL_OVERTEMPn
FAN_CTRL_OVERTEMPn
DEBUG0
DEBUG1
DEBUG2
DEBUG3
DEBUG4
DEBUG5
DEBUG15
16 BANK0_VRP
BANK0_VRP
DEBUG8
DEBUG9
DEBUG10
DEBUG11
DEBUG12
DEBUG13
DEBUG14
16 BANK0_VRN
BANK0_VRN
16 ENET_MDC
16 ENET_MDIO
16 ENET_TX_CLK
16 ENET_TX_EN
16 ENET_TXSLEW1
16 ENET_TX_D2
16 ENET_CRS
16 ENET_TX_D1
16 ENET_TX_D0
16 ENET_TXSLEW0
16 ENET_RX_ER
16 ENET_RX_CLK
16 ENET_RX_DV
16 ENET_RX_D0
16 ENET_RX_D1
16 ENET_RX_D2
16 ENET_RX_D3
ENET_MDC
ENET_MDIO
ENET_TX_CLK
ENET_TX_EN
ENET_TXSLEW1
ENET_TX_D2
ENET_CRS
ENET_TX_D1
ENET_TX_D0
ENET_TXSLEW0
ENET_RX_ER
ENET_RX_CLK
ENET_RX_DV
ENET_RX_D0
ENET_RX_D1
ENET_RX_D2
ENET_RX_D3
Rice University
Title
WARP FPGA Board
Description
Misc FPGA I/O
Rev
1.1
Date: Friday, December 16, 2005
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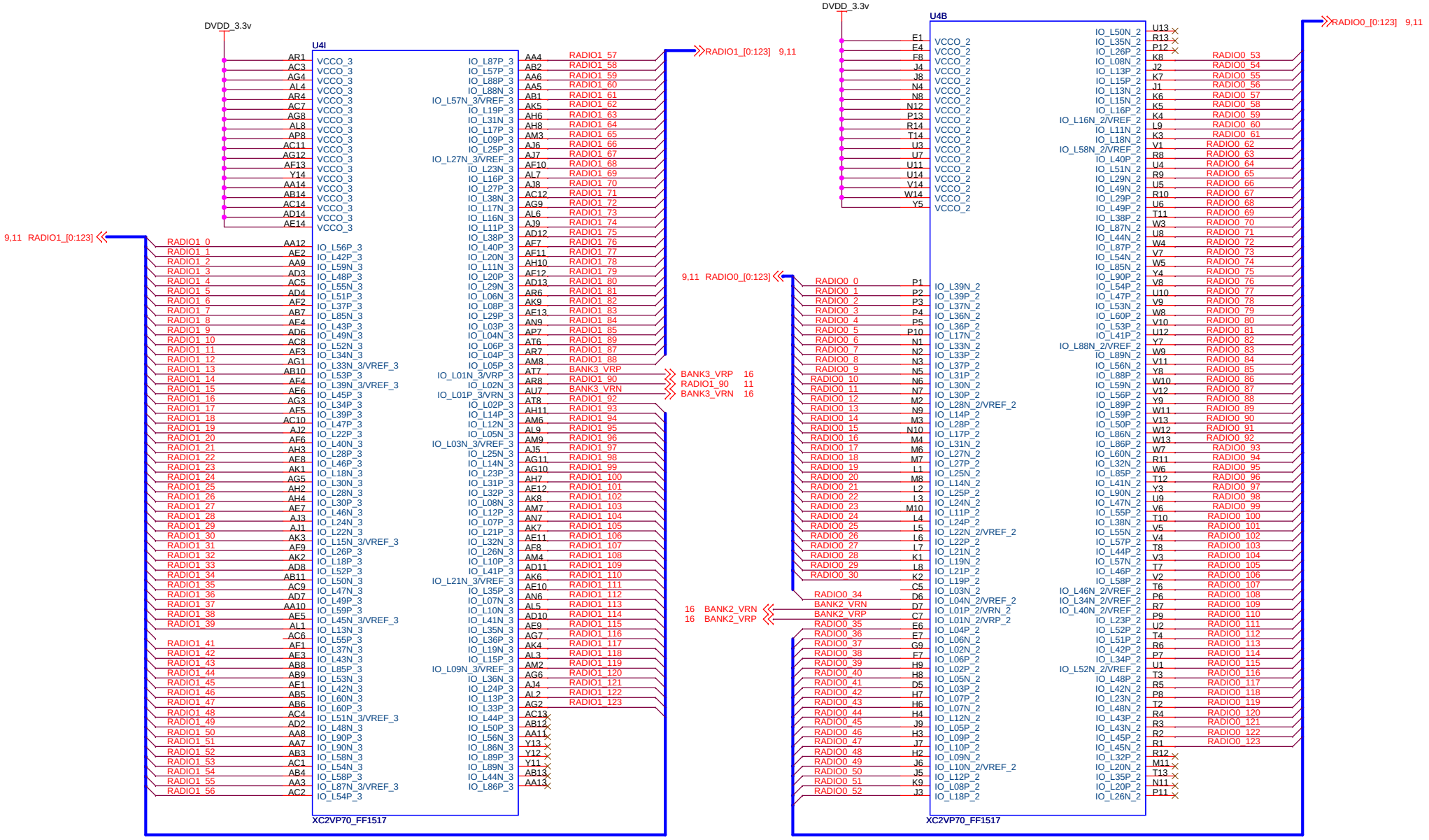

Rice University	
Title: WARP FPGA Board	
Description: Daughtercards 0-1 FPGA I/O	Rev: 1.1
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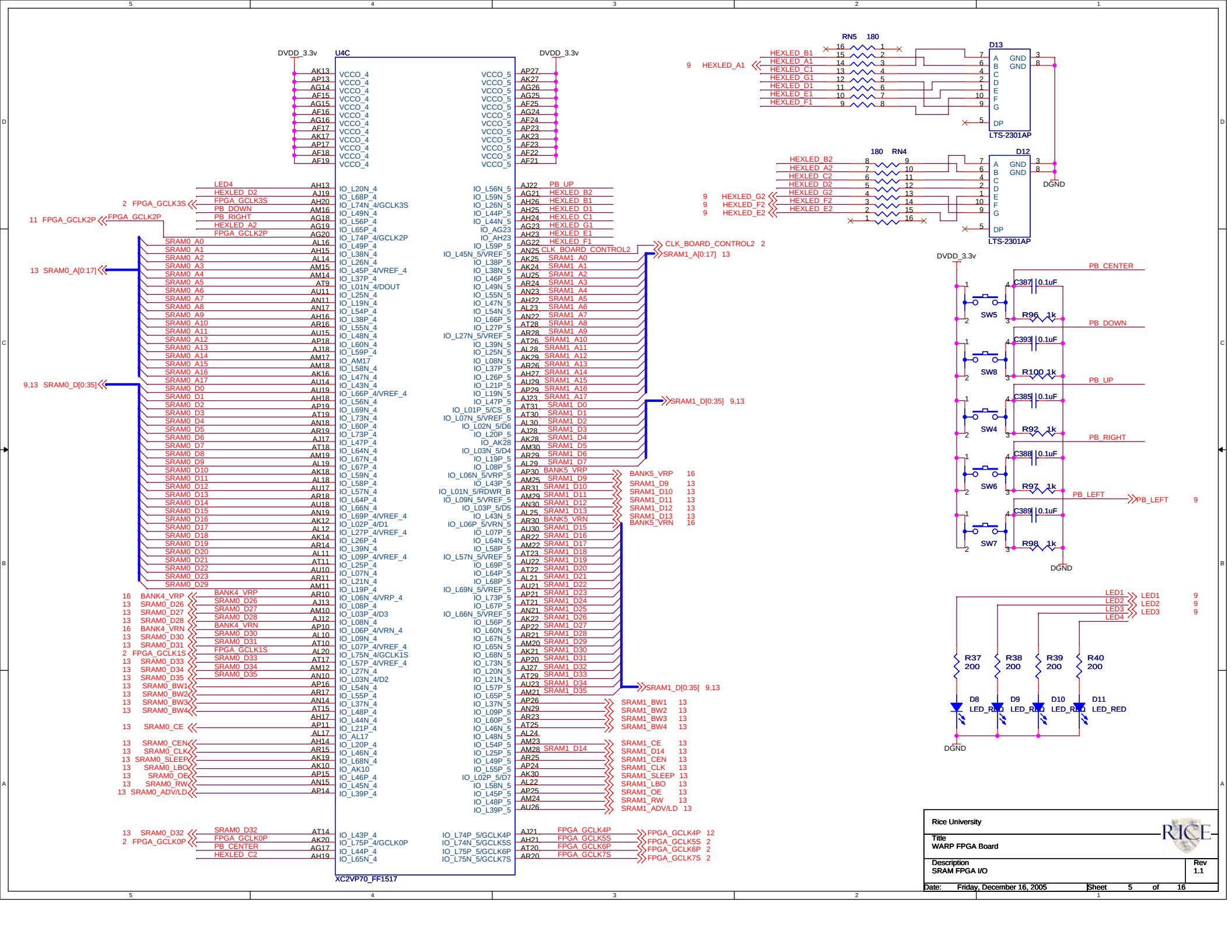
DVDD_3.3v
U4C
XC2VP70_FF1517
VCCO_4
VCCO_5
LED4
HEXLED_D2
FPGA_GCLK3S
PB_DOWN
PB_RIGHT
HEXLED_A2
FPGA_GCLK2P
SRAM0_A[0:17]
SRAM0_D[0:35]
BANK4_VRP
BANK4_VRN
FPGA_GCLK1S
SRAM0_CE
SRAM0_CEN
SRAM0_CLK
SRAM0_SLEEP
SRAM0_LBO
SRAM0_OE
SRAM0_RW
SRAM0_ADV/LD
SRAM0_D32
FPGA_GCLK0P
PB_CENTER
HEXLED_C2
PB_UP
HEXLED_B2
HEXLED_B1
HEXLED_D1
HEXLED_C1
HEXLED_G1
HEXLED_E1
HEXLED_F1
CLK_BOARD_CONTROL2
SRAM1_A[0:17]
SRAM1_D[0:35]
BANK5_VRP
BANK5_VRN
SRAM1_BW1
SRAM1_BW2
SRAM1_BW3
SRAM1_BW4
SRAM1_CE
SRAM1_D14
SRAM1_CEN
SRAM1_CLK
SRAM1_SLEEP
SRAM1_LBO
SRAM1_OE
SRAM1_RW
SRAM1_ADV/LD
FPGA_GCLK4P
FPGA_GCLK5S
FPGA_GCLK6P
FPGA_GCLK7S
RN5 180
RN4 180
HEXLED_A1
HEXLED_G2
HEXLED_F2
HEXLED_E2
D13
D12
LTS-2301AP
DGND
PB_CENTER
PB_DOWN
PB_UP
PB_RIGHT
PB_LEFT
SW5
SW8
SW4
SW6
SW7
C387 0.1uF
C393 0.1uF
C385 0.1uF
C388 0.1uF
C389 0.1uF
R96 1k
R100 1k
R92 1k
R97 1k
R98 1k
LED1
LED2
LED3
LED4
R37 200
R38 200
R39 200
R40 200
D8 LED_RED
D9 LED_RED
D10 LED_RED
D11 LED_RED
Rice University
Title
WARP FPGA Board
Description
SRAM FPGA I/O
Rev
1.1
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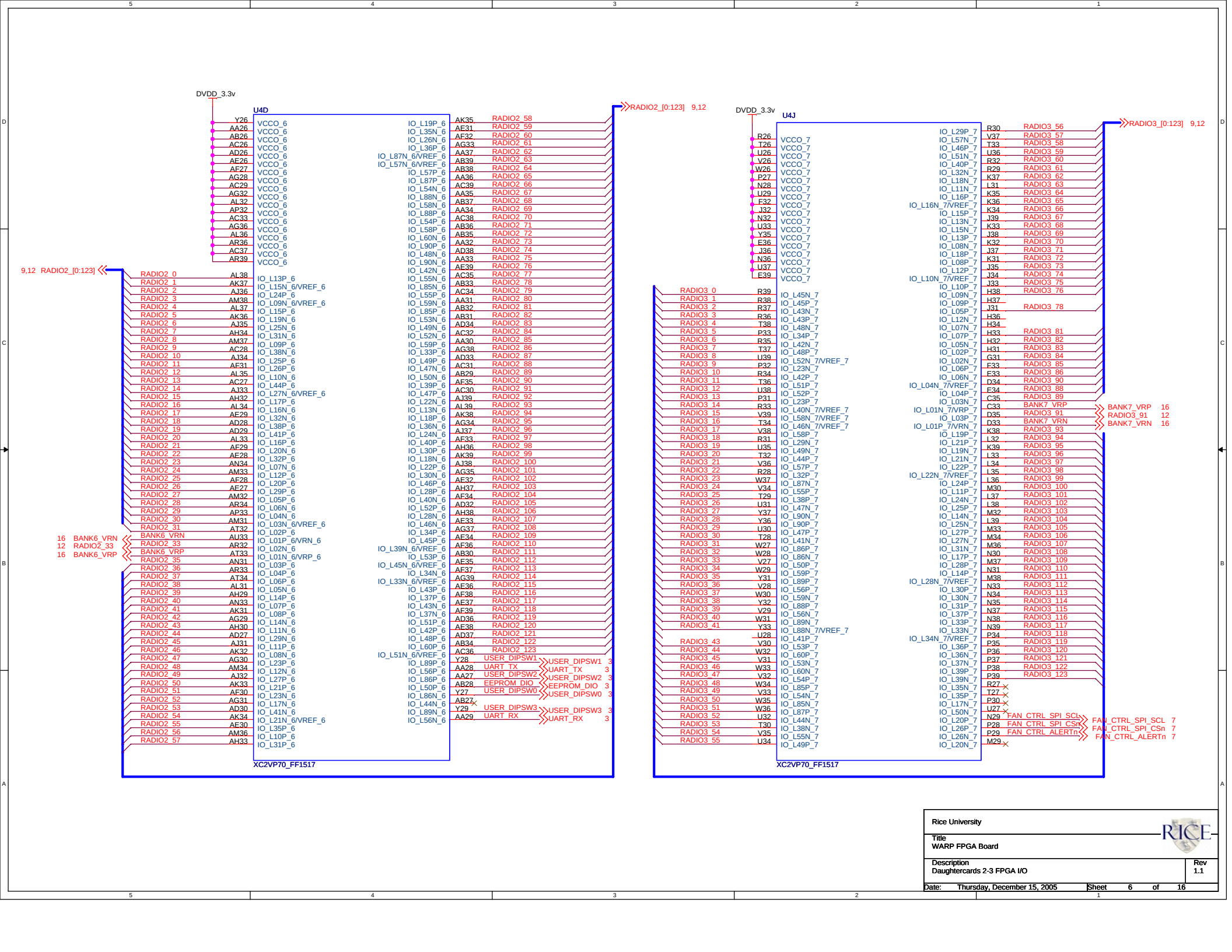

Rice University	
Title: WARP FPGA Board	
Description: Daughtercards 2-3 FPGA I/O	Rev: 1.1
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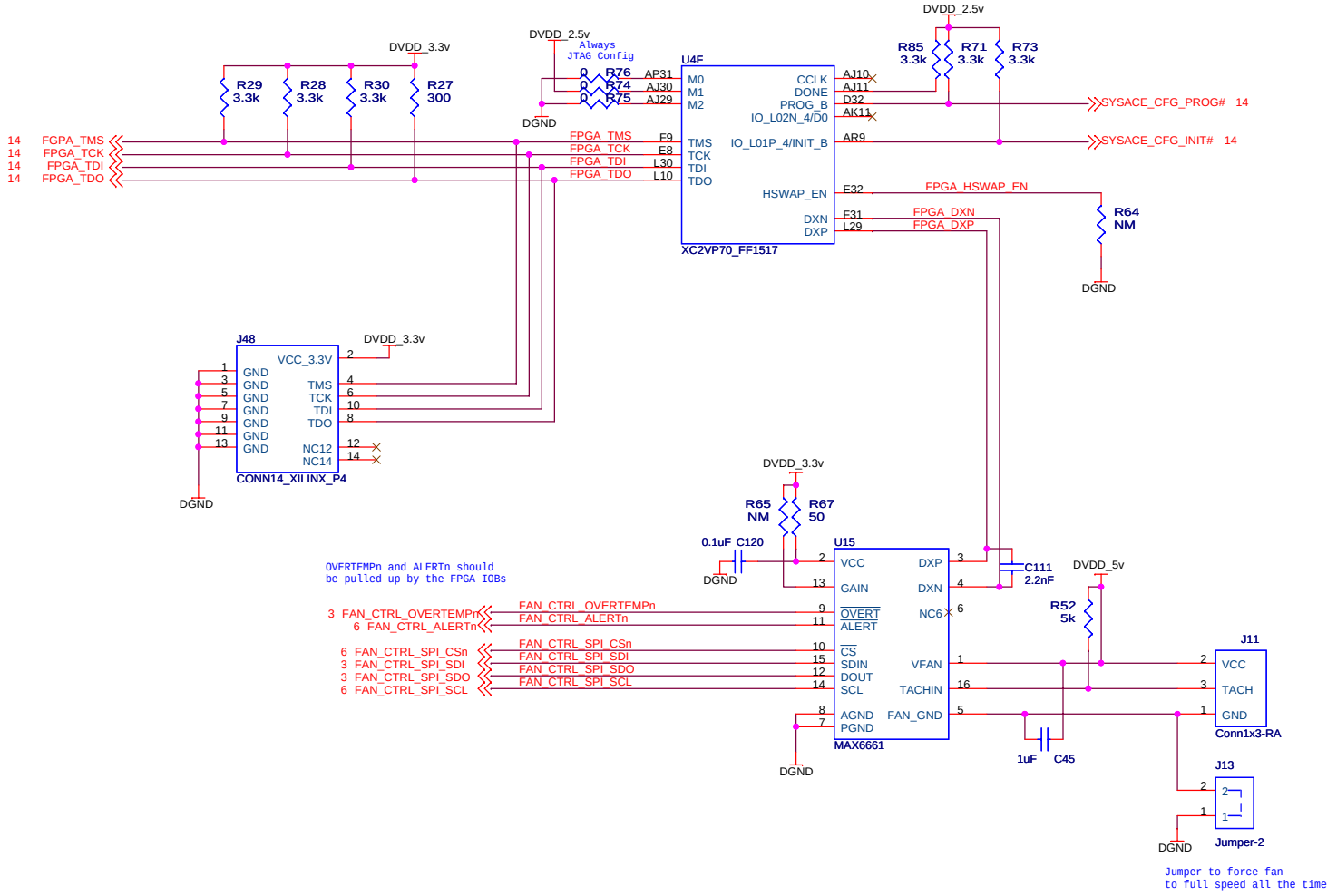

Rice University	
Title: WARP FPGA Board	
Description: FPGA JTAG, Configuration & Temperature Control	Rev: 1.1
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Notes:
MGTB_AGND: Analog ground for bottom edge MGTs
MGTT_AGND: Analog ground for top edge MGTs
MGT_2.5v: Dedicated MGT power supply
MGT_VTR_x: MGT Rx termination voltage
(tied to MGT_2.5v for DC coupling, 1.8v for AC)

DVDD_2.5v

Unused MGTs must still be powered
See pg. 14 of the V2Pro Datasheet for details

U4E

Bottom Edge MGTs

Top Edge MGTs

XC2VP70_FF1517

MGT_2.5v

MGT_VTR_1 MGT_VTR_2 MGT_VTR_3 MGT_VTR_4 MGT_VTR_5 MGT_VTR_6 MGT_VTR_7 MGT_VTR_8

MGT_1.8v

MGTB_AGND

MGTT_AGND

HSSDC2 Jack

Molex: 74703-0007
Mouser: Stock 10/31

Four MGTs always set for DC-coupled links
Four MGTs configurable for AC or DC-coupled links

Analog/Digital Ground Filtering

Top MGTs are used, so copule their AGND through inductors

L23 PLM18AG102SN1
L5 PLM18AG102SN1
L18 PLM18AG102SN1
L43 PLM18AG102SN1
L2 PLM18AG102SN1

Bottom MGTs are unused, so their AGND is just DGND

MGTB_AGND DGND MGTT_AGND DGND

Rice University	
Title: WARP FPGA Board	
Description: Multi-gigabit Transceivers	Rev: 1.1
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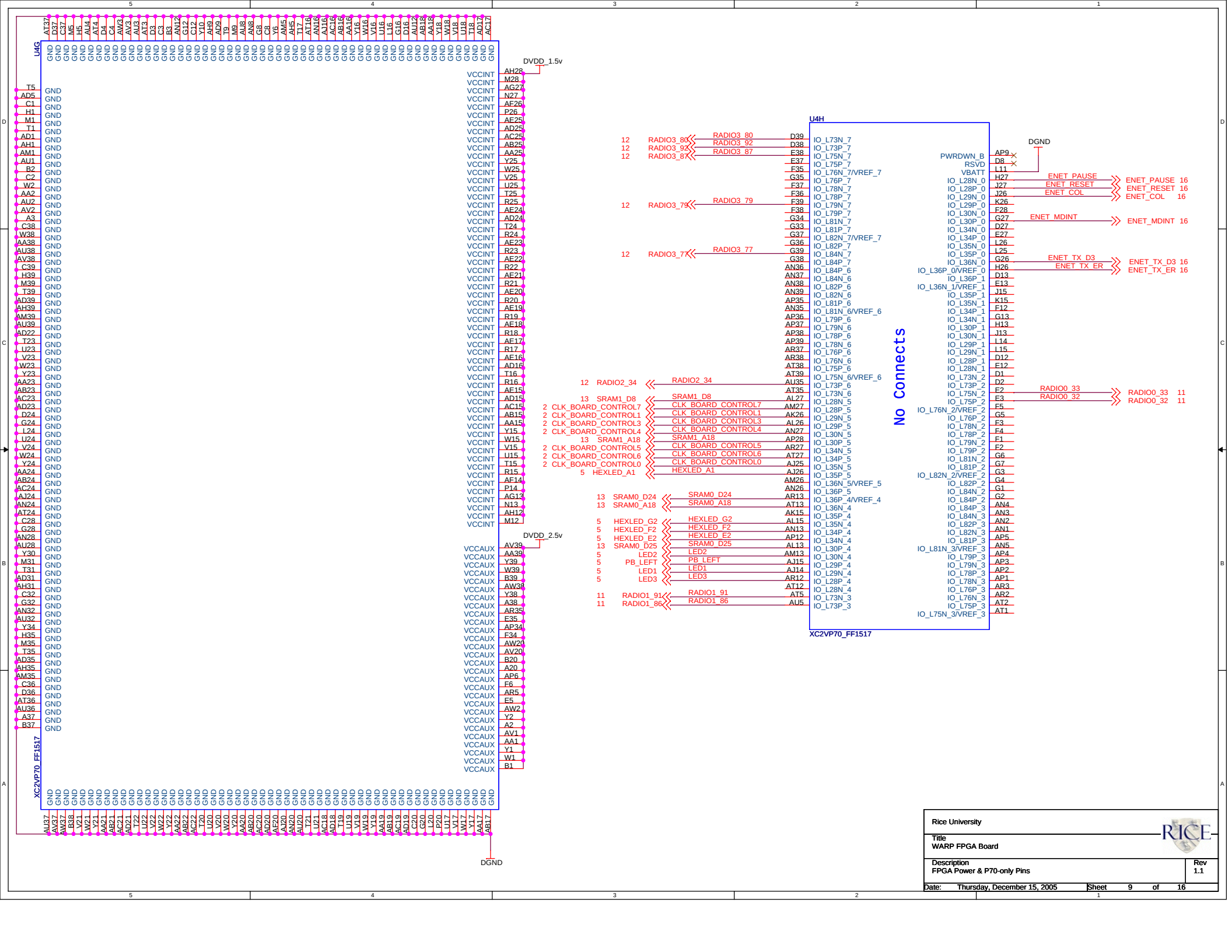
U4G
XC2VP70_FF1517
DVDD_1.5v
DVDD_2.5v
DGND
U4H
XC2VP70_FF1517
No Connects
RADIO3_80
RADIO3_92
RADIO3_87
RADIO3_79
RADIO3_77
RADIO2_34
SRAM1_D8
CLK_BOARD_CONTROL7
CLK_BOARD_CONTROL1
CLK_BOARD_CONTROL3
CLK_BOARD_CONTROL4
SRAM1_A18
CLK_BOARD_CONTROL5
CLK_BOARD_CONTROL6
CLK_BOARD_CONTROL0
HEXLED_A1
SRAM0_D24
SRAM0_A18
HEXLED_G2
HEXLED_F2
HEXLED_E2
SRAM0_D25
LED2
PB_LEFT
LED1
LED3
RADIO1_91
RADIO1_86
ENET_PAUSE
ENET_RESET
ENET_COL
ENET_MDINT
ENET_TX_D3
ENET_TX_ER
RADIO0_33
RADIO0_32
Rice University
Title
WARP FPGA Board
Description
FPGA Power & P70-only Pins
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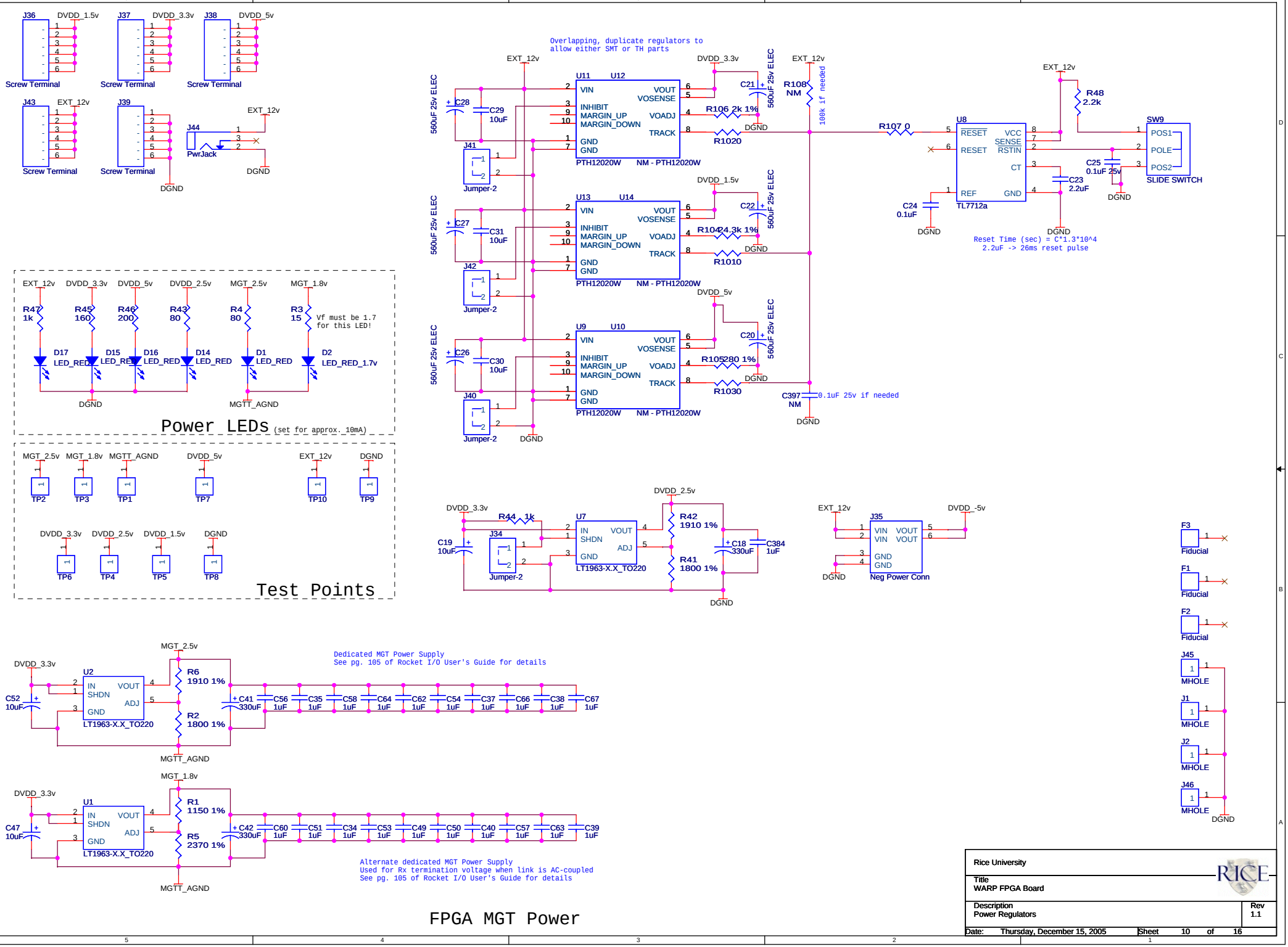
J36 DVDD_1.5v
J37 DVDD_3.3v
J38 DVDD_5v
Screw Terminal
J43 EXT_12v
J39
J44
PwrJack
DGND
Overlapping, duplicate regulators to allow either SMT or TH parts
EXT_12v
DVDD_3.3v
DVDD_1.5v
DVDD_5v
U11 U12
U13 U14
U9 U10
VIN
VOUT
VOSENSE
INHIBIT
MARGIN_UP
MARGIN_DOWN
VOADJ
TRACK
GND
PTH12020W NM - PTH12020W
560uF 25v ELEC
C28 C29 10uF
C27 C31 10uF
C26 C30 10uF
C21
C22
C20
R106 2k 1%
R1024.3k 1%
R105280 1%
R1020
R1010
R1030
R108 NM
100k if needed
R107 0
C397 NM
0.1uF 25v if needed
Jumper-2
J41
J42
J40
U8
TL7712a
RESET
VCC
SENSE
RSTIN
CT
REF
R48 2.2k
C25 0.1uF 25v
C23 2.2uF
C24 0.1uF
SW9
SLIDE SWITCH
POS1
POLE
POS2
Reset Time (sec) = C*1.3*10^4
2.2uF -> 26ms reset pulse
Power LEDs (set for approx. 10mA)
MGT_2.5v
MGT_1.8v
DVDD_2.5v
R47 1k
R45 160
R46 200
R43 80
R4 80
R3 15
Vf must be 1.7 for this LED!
D17 LED_RED
D15 LED_RED
D16 LED_RED
D14 LED_RED
D1 LED_RED
D2 LED_RED_1.7v
MGTT_AGND
Test Points
TP2
TP3
TP1
TP7
TP10
TP9
TP6
TP4
TP5
TP8
U7
LT1963-X.X_TO220
IN
SHDN
GND
VOUT
ADJ
R44 1k
R42 1910 1%
R41 1800 1%
C19 10uF
C18 330uF
C384 1uF
J34
J35
Neg Power Conn
DVDD_-5v
F3
F1
F2
Fiducial
J45
J1
J2
J46
MHOLE
U2
R6 1910 1%
R2 1800 1%
C52 10uF
C41 330uF
C56 C35 C58 C64 C62 C54 C37 C66 C38 C67 1uF
Dedicated MGT Power Supply
See pg. 105 of Rocket I/O User's Guide for details
U1
R1 1150 1%
R5 2370 1%
C47 10uF
C42 330uF
C60 C51 C34 C53 C49 C50 C40 C57 C63 C39 1uF
Alternate dedicated MGT Power Supply
Used for Rx termination voltage when link is AC-coupled
See pg. 105 of Rocket I/O User's Guide for details
FPGA MGT Power
Rice University
Title
WARP FPGA Board
Description
Power Regulators
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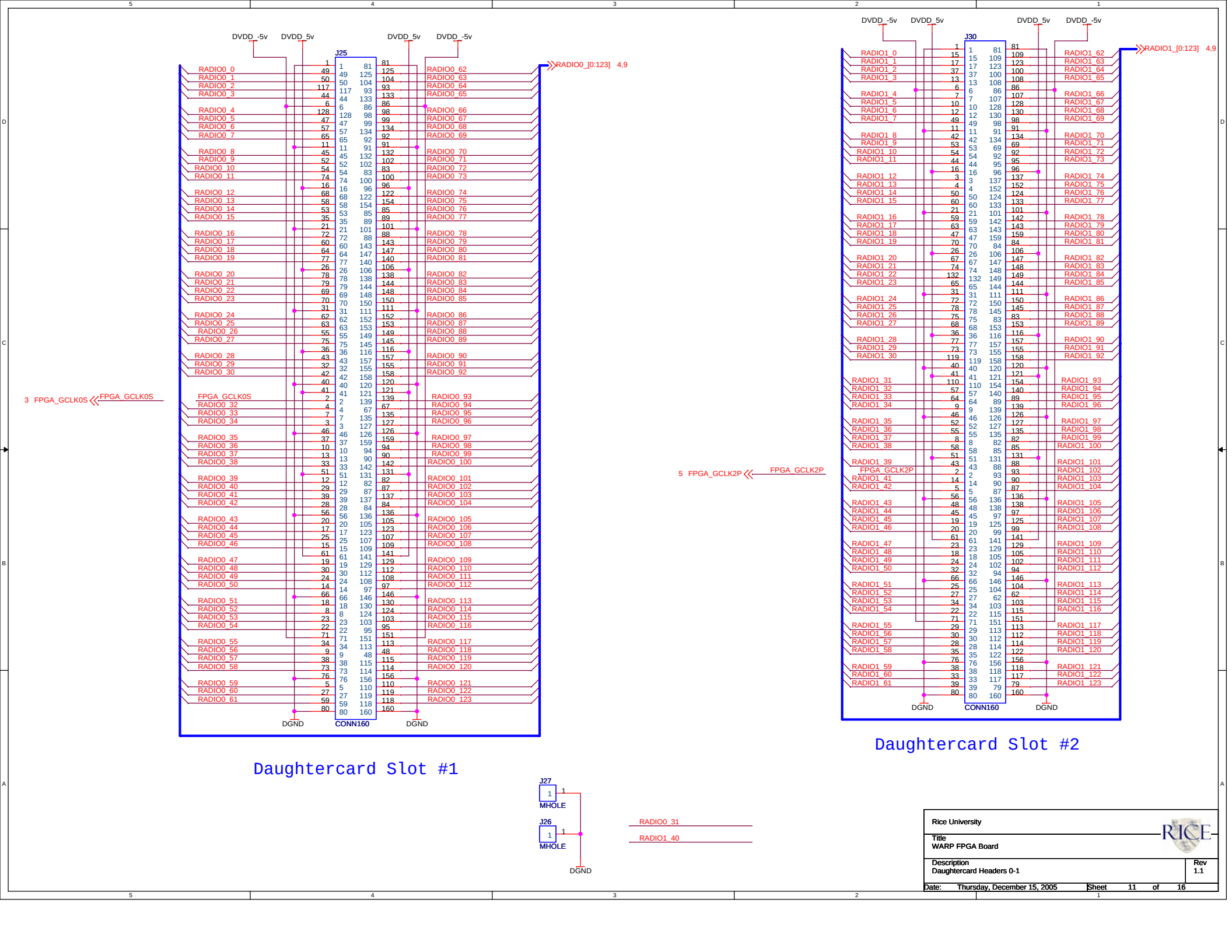
DVDD_-5v
DVDD_5v
J25
RADIO0_[0:123] 4,9
3 FPGA_GCLK0S
FPGA_GCLK0S
DGND
CONN160
Daughtercard Slot #1
J30
RADIO1_[0:123] 4,9
5 FPGA_GCLK2P
FPGA_GCLK2P
Daughtercard Slot #2
J27
MHOLE
J26
RADIO0_31
RADIO1_40
Rice University
Title
WARP FPGA Board
Description
Daughtercard Headers 0-1
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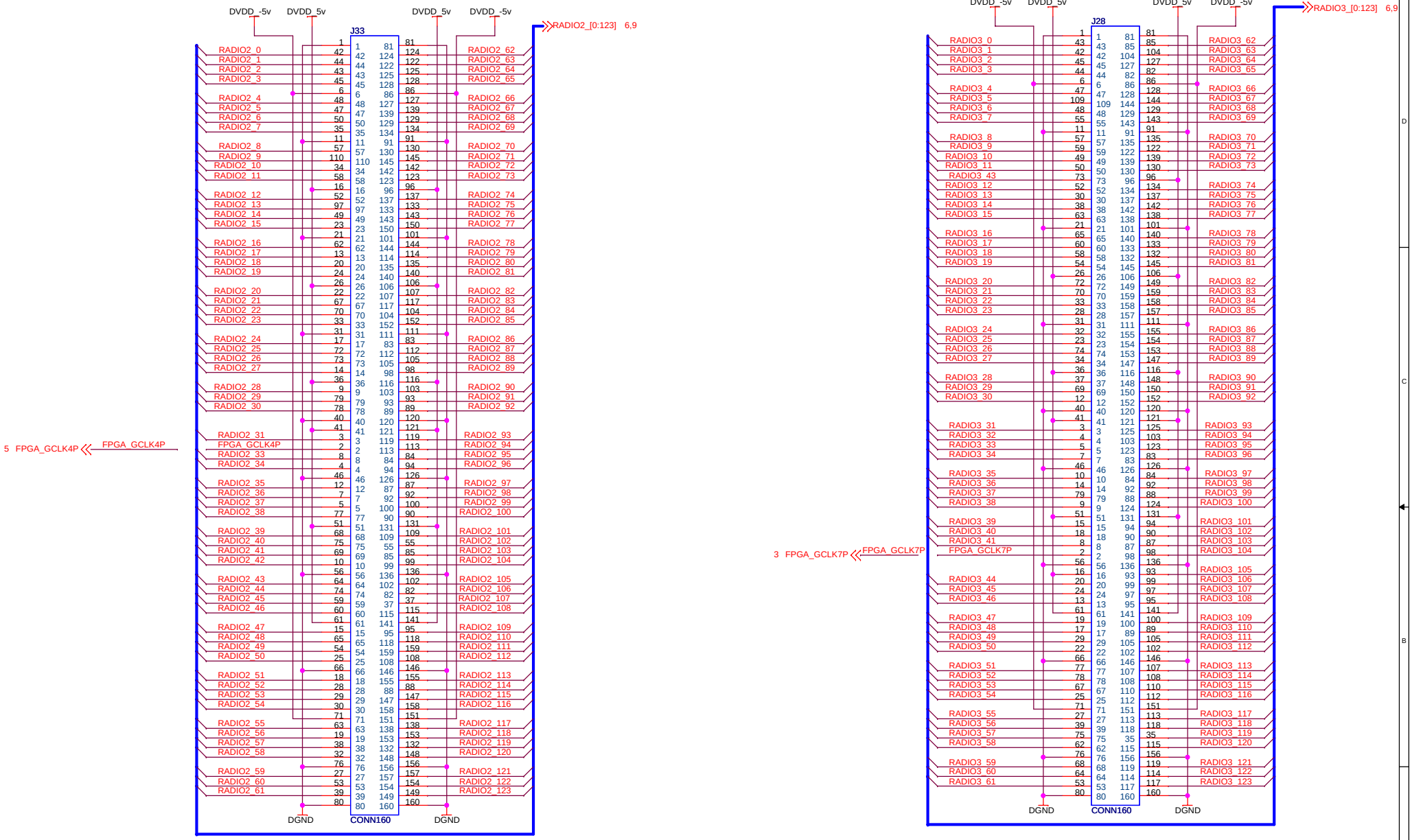
DVDD_-5v
DVDD_5v
DVDD_5v
DVDD_-5v
RADIO2_[0:123] 6,9
J33
CONN160
DGND
DGND
RADIO2_0
RADIO2_1
RADIO2_2
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DVDD_5v
DVDD_-5v
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DGND
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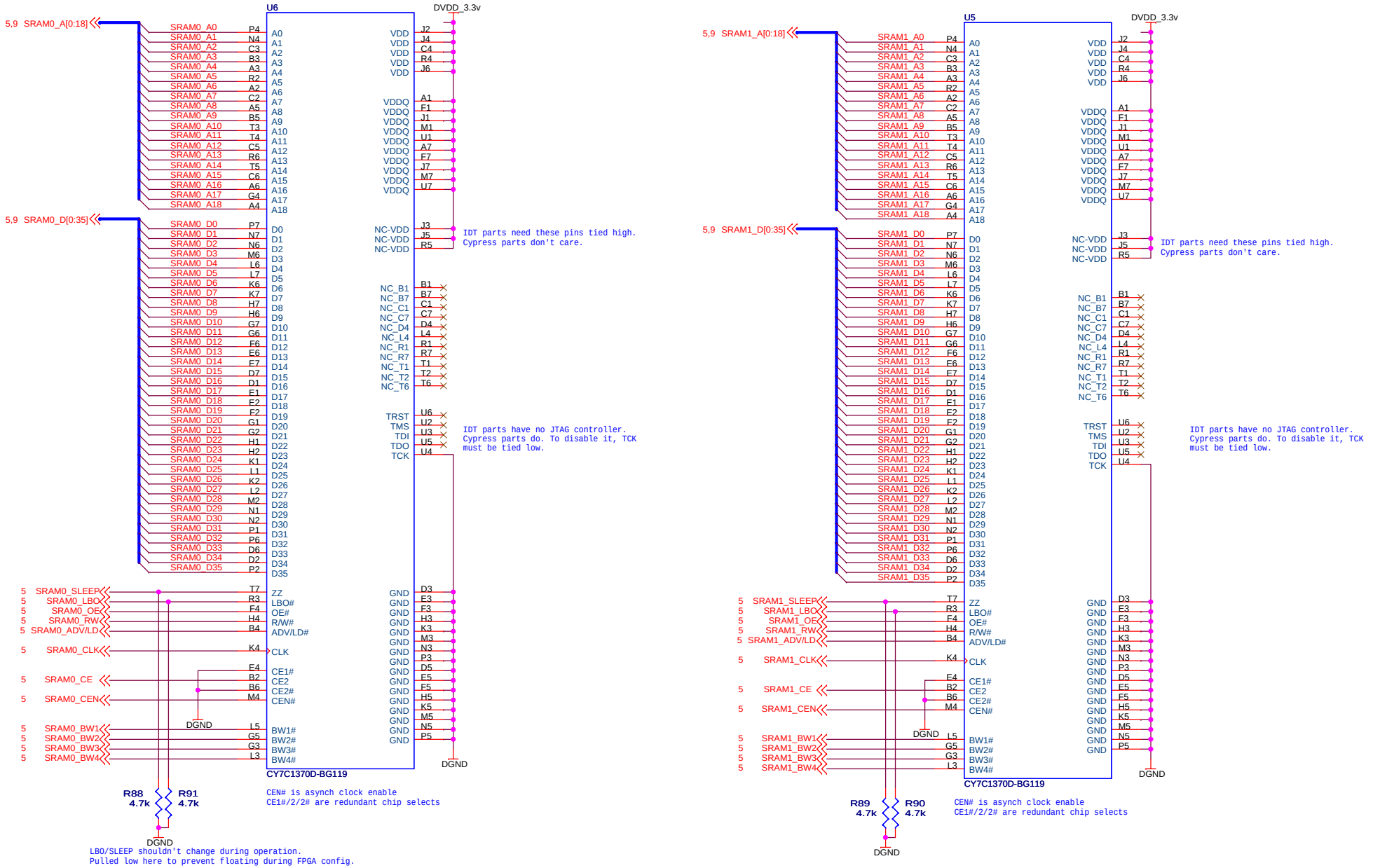
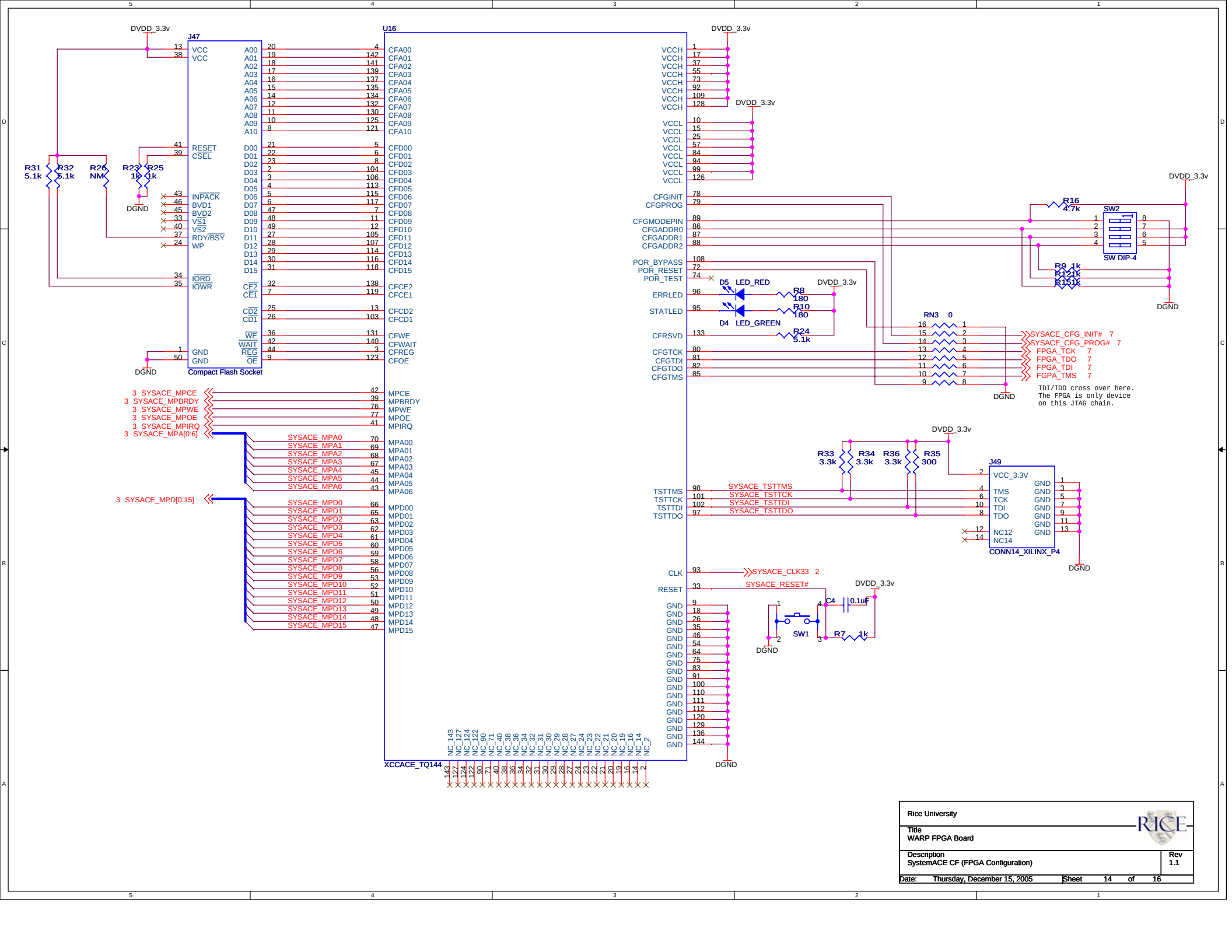
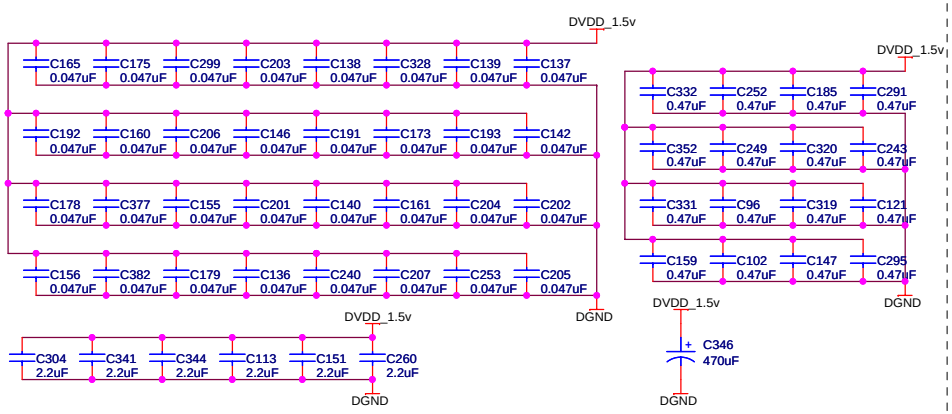
3 FPGA_GCLK7P
FPGA_GCLK7P
Daughtercard Slot #4
Rice University
Title
WARP FPGA Board
Description
Daughtercard Headers 2-3
Rev
1.1
Date: Thursday, December 15, 2005
Sheet 12 of 16



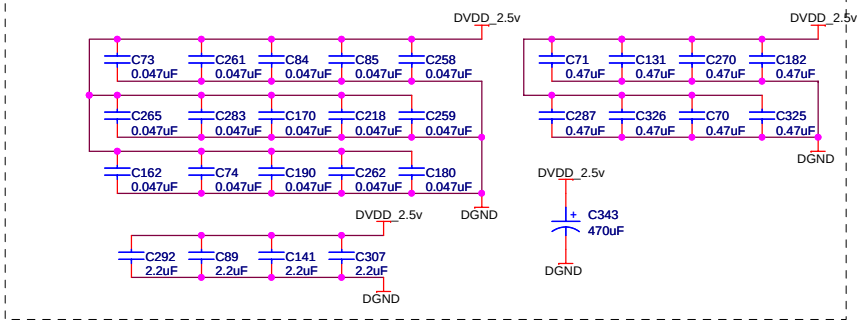
Rice University	
Title: WARP FPGA Board	
Description: SRAMs	Rev: 1.1
Date: Thursday, December 15, 2005	Sheet 13 of 16


DVDD_3.3v
J47
U16
Compact Flash Socket
XCCACE_TQ144
DGND
R31 5.1k
R32 5.1k
R26 NM
R23 1k
R25 1k
R16 4.7k
SW2
SW DIP-4
R9 1k
R12 1k
R15 1k
D5 LED_RED
D4 LED_GREEN
R8 180
R10 180
R24 5.1k
RN3 0
SYSACE_CFG_INIT# 7
SYSACE_CFG_PROG# 7
FPGA_TCK 7
FPGA_TDO 7
FPGA_TDI 7
FGPA_TMS 7
TDI/TDO cross over here.
The FPGA is only device
on this JTAG chain.
R33 3.3k
R34 3.3k
R36 3.3k
R35 300
J49
VCC_3.3V
CONN14_XILINX_P4
SW1
C4 0.1uF
R7 1k
SYSACE_CLK33 2
SYSACE_RESET#
3 SYSACE_MPCE
3 SYSACE_MPBRDY
3 SYSACE_MPWE
3 SYSACE_MPOE
3 SYSACE_MPIRQ
3 SYSACE_MPA[0:6]
3 SYSACE_MPD[0:15]
Rice University
WARP FPGA Board
SystemACE CF (FPGA Configuration)
Rev 1.1
Date: Thursday, December 15, 2005
Sheet 14 of 16

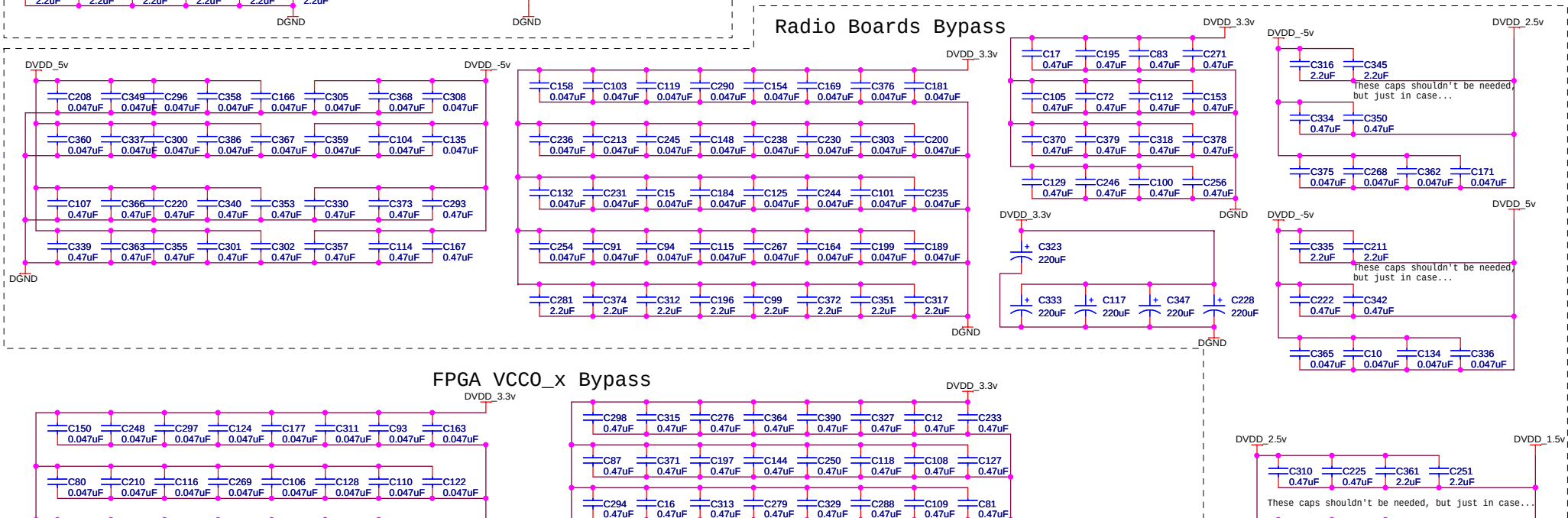
FPGA VCC_INT Bypass (56 power pins)



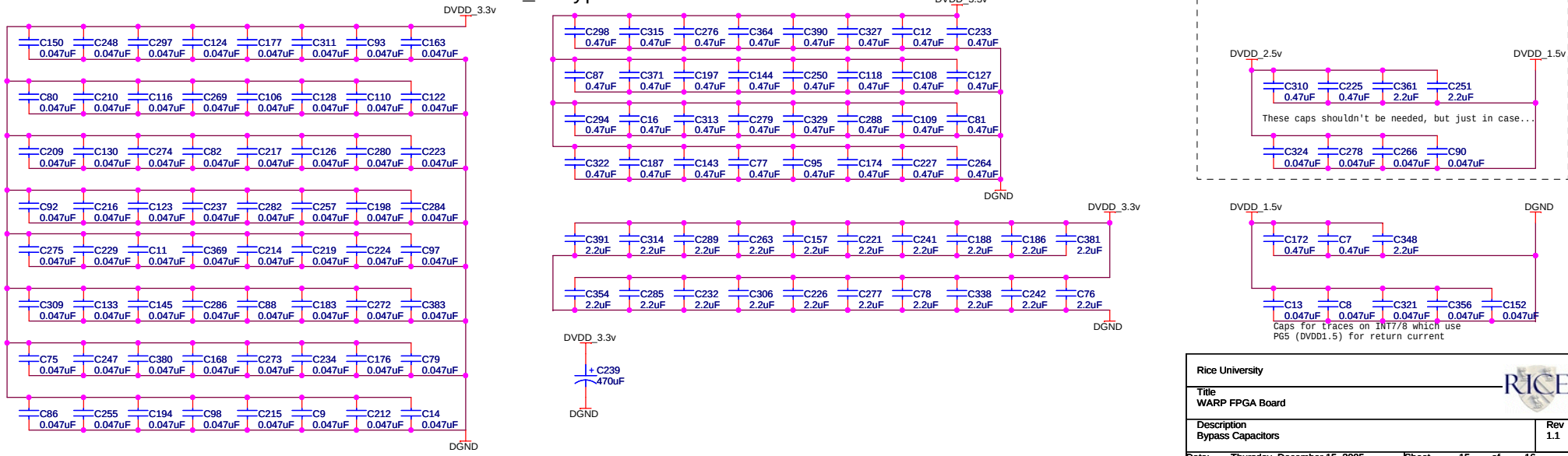
FPGA VCC_AUX Bypass (28 power pins)



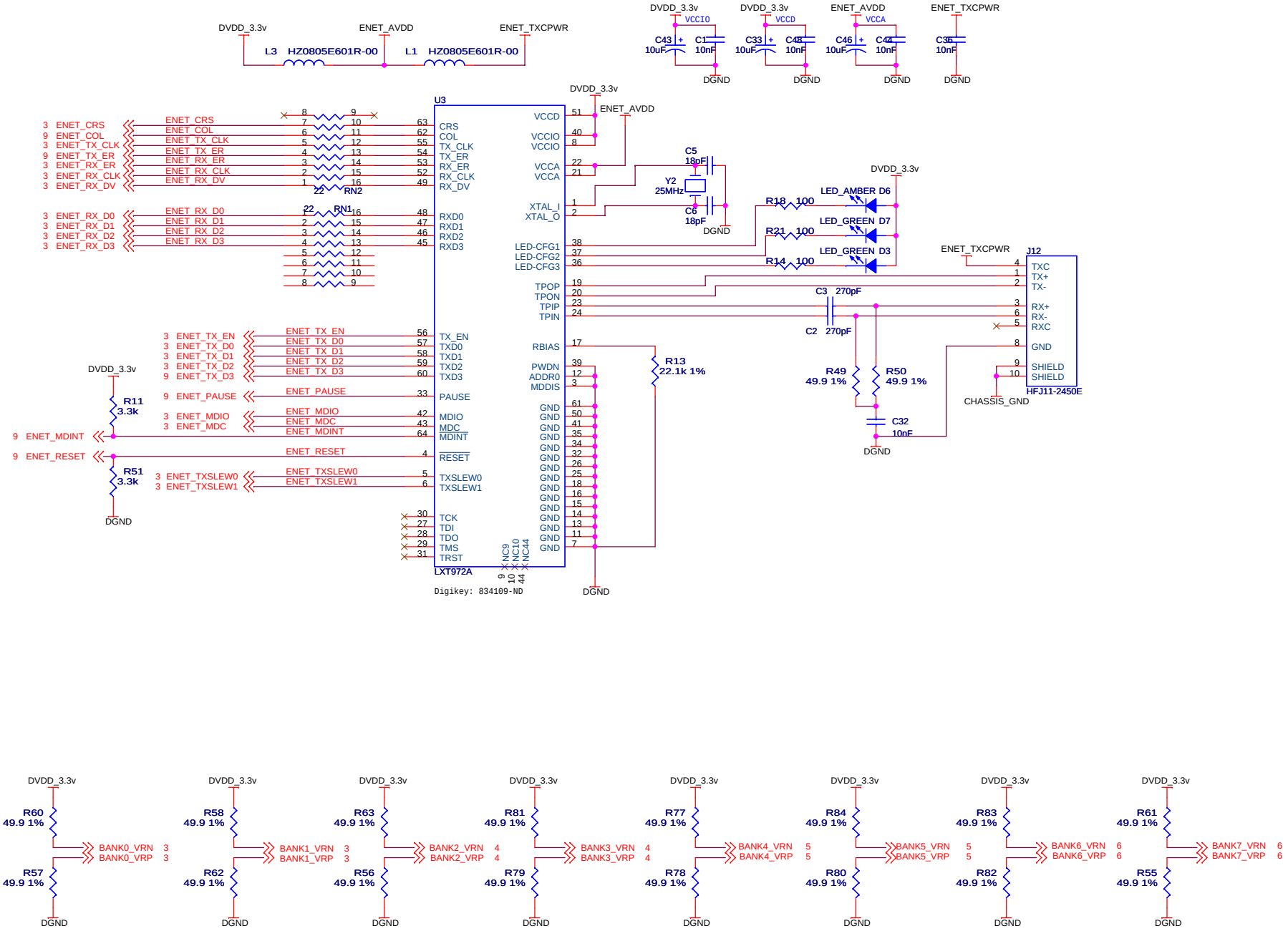
Radio Boards Bypass



FPGA VCCO_x Bypass



Rice University		
Title: WARP FPGA Board		
Description: Bypass Capacitors		Rev: 1.1
Date: Thursday, December 15, 2005	Sheet 15 of 16	



Digitally Controlled Impedance Reference Resistors
Every I/O bank has option of 50-ohm DCI

When using DCI, the Bitgen option "DCI Update Mode"
should *not* be set to Quiet. If it is, some I/O will not
function properly. See pg. 235 of the Virtex-II Pro
User's Guide (DCI section of ug012.pdf) for more information

Rice University	
Title: WARP FPGA Board	
Description: 10/100 Ethernet PHY and DCI Resistors	Rev: 1.1
Date: Thursday, December 15, 2005	Sheet 16 of 16